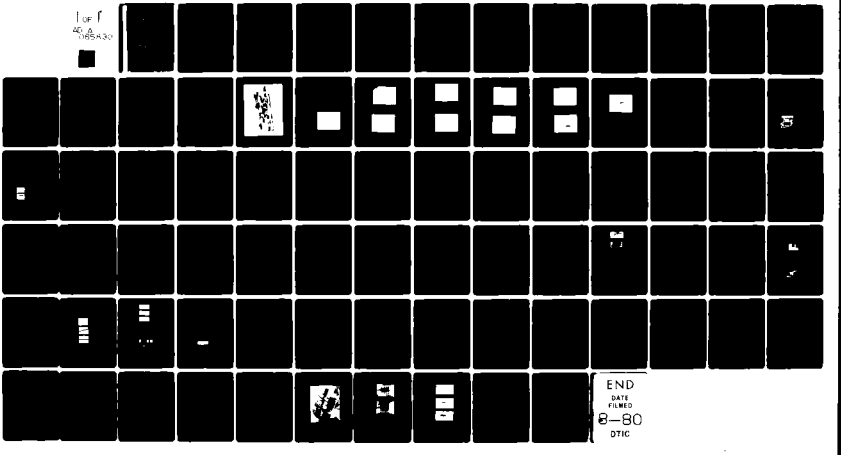
AD-A085 830 RCA LABS PRINCETON NJ F/G 9/5
DUAL-GATE MESFET VARIABLE-GAIN CONSTANT-OUTPUT POWER AMPLIFIER.(U)
APR 80 M KUMAR N00173-78-C-0227
UNCLASSIFIED PRRL-80-CR-12 NL



END
DATE FILMED
8-80
DTIC

(12)

(6) DUAL-GATE MESFET VARIABLE-GAIN CONSTANT-OUTPUT POWER AMPLIFIER

(12) Mahesh [redacted] Kumar
RCA Laboratories
Princeton, New Jersey 08540

(11) APR [redacted] 80 (12) 77

(9) FINAL REPORT
for the period 18 Sep [redacted] 78 to 17 Mar [redacted] 80

(14) PRRL-80-CR-12

Prepared for
Naval Research Laboratory
Washington, DC 20375

(15) Contract No. N00173-78-C-0227

299000

80 6 25 00

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO. AD-A086830	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) DUAL-GATE MESFET VARIABLE-GAIN, CONSTANT-OUTPUT POWER AMPLIFIER	5. TYPE OF REPORT & PERIOD COVERED FINAL REPORT (9-18-78 to 3-17-80)
	6. PERFORMING ORG. REPORT NUMBER PRRL-80-CR-12
7. AUTHOR(s) M. Kumar	8. CONTRACT OR GRANT NUMBER(s) N00173-78-C-0227
9. PERFORMING ORGANIZATION NAME AND ADDRESS RCA Laboratories Princeton, New Jersey 08540	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Research Laboratory Washington, DC 20375	12. REPORT DATE April 1980 13. NUMBER OF PAGES 77
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Variable-gain microwave amplifier
Microwave amplifier
Dual-gate MESFET
Limiter
Microwave AGC amplifier
Phase I of this study

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This final report describes the development of a variable-gain, constant-output power amplifier. The program was divided into two phases. Phase I proved the feasibility of the variable-gain, constant-output power amplifier from the chosen approach by demonstrating a breadboard model. This work was reported in Bimonthly Report No. 6 (Appendix F). Phase II of this program was

(over)

DD FORM 1 JAN 73 1473

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

299

During Phase II, the development

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20.

to develop the final packaged amplifier with improved performance. During this phase, the following tasks were completed: (1) a dual-gate FET amplifier was redesigned to obtain more gain (10 dB) over the band; (~~ii~~ 2) a video amplifier was designed and developed for higher gain (40 dB); and (~~iii~~ 3) circulators were eliminated to reduce the size of the amplifier.

This amplifier was demonstrated to operate over a 3-GHz band (4.5 to 7.5 GHz) and to provide an output power of 3 ±2 dBm over its entire dynamic range of -45 to 0 dBm of input power.

The linear AGC amplifier developed under this program has the following key features. (1) It preserves amplitude modulation of the incoming signal. (2) It can perform normal AGC function under a multiple-pulse condition. This characteristic may prove to be very useful for handling multiple threats. (3) It is very versatile. It can provide separate ports to facilitate output power level adjustment and input signal detection and monitoring. (4) It has very fast response. The rise time and fall time of this amplifier are better than 15 ns which is limited by the measurement system.

The program has been successfully completed by delivering the breadboard and final packaged amplifiers meeting essentially all contract goals.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

PREFACE

This final report describes work performed in the Microwave Technology Center of RCA Laboratories during the period 18 September 1978 to 17 March 1980 under Contract No. N00173-78-C-0227. The Center's director is F. Sterzer, and H. C. Huang is the group head. M. Kumar is the project scientist. Also participating in this program were D. W. Bechtle and S. A. Siegel. The assembly work was performed by E. Mykietyn and P. A. Czajkowski.

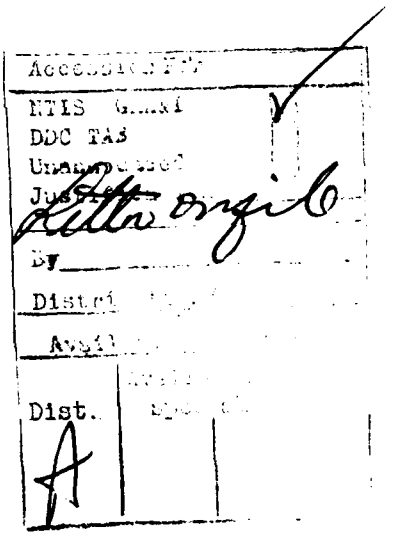


TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION I

INTRODUCTION

The objective of this program is the development of a linear automatic gain control (AGC) constant-output power amplifier with following specifications:

Frequency:	4 to 8 GHz
Bandwidth:	3 GHz
Noise Figure:	7 dB
Power Output:	0 dBm (min)
Output-Power Variation:	±1 dB (max)
Dynamic Range:	-50 to 0 dBM, power input
Response Time:	<1 ns

The amplifier is required to have provisions for the following functions:

(1) The output rf power level of the amplifier should be settable by an externally supplied dc input voltage.

(2) A separate port for direct amplifier cut-off and video gain control (pulsed control signal).

(3) A separate output port for supplying a video output signal derived from the amplifier feedback leveling control.

A. APPLICATIONS

The AGC, constant-output power FET amplifier developed in this program has a large number of system applications which require an input amplifier with the capacity to handle a large dynamic signal range with variable gain and constant rf power output with extremely fast response. Some of these applications are cited below to indicate the general utility of the variable-gain, constant-output power amplifier which has an advantage over the conventional limiter by being capable of preserving amplitude modulation and phase coherence on a wide dynamic signal strength range.

1. Radar Receiver - Front End Applications

Long-range radars are subjected to a wide variation in received echo signals. The signal strength, which varies inversely as the fourth power of distance, requires a programmed sensitivity time control (STC) of the gain.

With STC, strong "up-close" reflected signals cannot overload the amplifier because the gain is automatically programmed with time to increase appreciably to accommodate weak signals. Automated gain control as a function of time provides good results for stationary, uniform targets. However, the STC approach alone does not provide for gain control on the basis of the effective radar target cross-section or random intercepted signals which can jam the radar.

The FET AGC amplifier lends itself to automated STC gain control while guarding against large amplitude signals that might overload the receiver. Variability of gain (AGC) purely on the basis of intercepted signal strength maintains optimum receiver sensitivity at all times with the capability of responding to lower gain level requirements within 30 ns.

2. ESM Receiver

The amplitude content or video signature of the cw or pulsed signal received by the electronic surveillance measurements (ESM) system can be of significant importance. The amplitude of the radar pulse may be coded to enable automatic recognition of the returned echo and to thwart jamming. Therefore, as a countermeasure against an amplitude-coded radar pulse, the jamming transmitter must be similarly amplitude modulated. This modulation must, therefore, be detected and preserved by the countermeasure receiver. A conventional limiter amplifier does not have this capability.

The variable-gain, constant-output amplifier will preserve the video amplitude coding of the radar pulse. This amplitude preservation is assured because the automatic gain adjustment will prevent saturation of the amplifier and amplitude clipping.

3. Preamplifier for Narrow Dynamic Range Receivers

The AGC amplifier will tolerate a 60-dB dynamic range and reduce this range to well under 10 dB at its output while still preserving AM, etc. This large reduction in average output power signal variation can be used to interface with and protect narrow dynamic input range receivers.

4. Burn-Out and Protection Capability

The fast response time of the AGC amplifier will enable attenuation of very large signals that would otherwise jeopardize and perhaps burn-out tunnel diode and bipolar amplifiers.

B. RCA BACKGROUND IN DUAL-GATE FET COMPONENTS

RCA has vast experience and background in the development of dual-gate FET components. We have already developed a two-stage dual-gate FET amplifier with small-signal gain of 20 ±0.75 dB, covering an octave bandwidth (4 to 8 GHz) and having a dynamic gain control range in excess of 60 dB (Appendix A). This amplifier has a switching (on-off) rise and fall time capability of about 100 ps. We have also developed and hold the basic patents of a dual-gate GaAs FET, as well as single-gate GaAs FET, power limiters (Appendices B, C, and D). The constant-output power independent of drive variations or frequency has been achieved by utilizing a multistage high-gain amplifier chain. The output stages of this amplifier operate in saturation regions where the output-power variations are greatly compressed, even for large variations in the input-power range. A novel wideband FET frequency discriminator has also been developed (Appendix E). This discriminator instantaneously covers the frequency range from 7 to 11 GHz, producing a dc output voltage ranging from approximately -200 mV at 7 GHz to +300 mV at 11 GHz for an input power of 0.2 mW.

C. PROGRAM SCOPE

The program was divided into two phases. Phase I was for demonstration of the feasibility of obtaining variable gain and constant output power on a breadboard model. Phase II requires the development of a final, packaged amplifier with provisions for processing input and output signals.

Phase I of this program was completed in September 1979 and the feasibility of obtaining variable gain and constant output power on a breadboard model was demonstrated. A breadboard amplifier was demonstrated operating over a 3-GHz band (4.5 to 7.5 GHz) and providing an output power of a 0 dBm ±2.5 dB over its dynamic range of -40 dBm to 0 dBm of input power. For any fixed input power level within that range, the output power variation is within ±1.5 dB. While the operation of the breadboard falls short of the ultimate program goal of a -50 to 0 dBm dynamic range and the output power of 0 dBm ±1 dB, the principle of a microwave AGC amplifier based on a dual-gate FET was nevertheless fully demonstrated. The progress of this breadboard amplifier development was reported in detail in Bimonthly Report No. 6 (see Appendix F).

This breadboard amplifier needed some improvements to meet the program goals: (1) improvement in the gain of the dual-gate FET amplifier and (2) design of a video amplifier with higher gain (40 dB). These improvements will allow us to use 10-dB couplers for sampling the rf power instead of 3-dB couplers used in the breadboard amplifier. Futhermore, the use of the rf amplifier in the AGC control unit can be eliminated. The video amplifier used in the commercial video control unit of the breadboard amplifier had a gain of only 25 dB.

Phase II of the program includes the redesign of the dual-gate FET amplifier and the video amplifier. This report covers the work performed during Phase II and includes a brief description of Phase I for the sake of completion. Phase II comprises three major tasks: (1) to design a dual-gate FET amplifier with more than 10-dB gain over the band; (2) to design the overall amplifier configuration for packaging; and (3) to develop a high-gain video amplifier. All these tasks were successfully completed and the performance of the final packaged amplifier was demonstrated. Following are the main features of the amplifier:

(1) It delivers constant output power (3 ±2 dBm) for any input power level from -45 to 0 dBm.

(2) It is a variable-gain, linear amplifier meaning that none of the stages run into saturation for the entire dynamic range of the input power. The gain of the amplifier is electronically controlled to track the input power level to keep output power constant.

(3) It preserves the amplitude modulation.

(4) It has a response time of better than 10 ns which is limited by our measurement system response time.

(5) It can detect two rf pulses separated by 10 ns of different amplitude (within its dynamic range) and delivers the output of the same amplitude (3 ±2 dBm).

(6) The output rf power level of the amplifier is settable by an externally supplied dc input voltage to the second gate of the final stage.

SECTION II

DESIGN OF DUAL-GATE FET AMPLIFIER

A single-stage amplifier was designed using an NEC* 46300 dual-gate FET. We measured the S-parameters of the FET and then designed the input and output matching circuits by CAD technique. These matching circuits were designed for realizing maximum gain from gate 1 to drain for a given drain and first-gate bias voltages with the second gate rf grounded. The circuit design used the COSMIC-S program developed at RCA Laboratories for optimizing the network design.

The measured S-parameters of a typical NEC 46300 dual-gate FET are shown in Table 1. Figure 1 shows the block diagram of the single-stage amplifier circuit. The variation of gain with second-gate bias voltage is shown in Fig. 2. The variation of gain with frequency for different second-gate bias voltage is shown in Fig. 3. As seen from Fig. 3, the single-stage amplifier has a gain of 10 dB minimum over 4.5 to 7.5 GHz. This is an improvement over the single-stage amplifier used in the breadboard model which had gains of 7 to 8 dB over the band.

TABLE 1. S-PARAMETERS OF NEC 46300 DEVICE BIAS V_o = 4 V, VG_1 = -1.3 V, VG_2 = 0 V

	S_{11}		S_{21}		S_{12}		S_{22}	
Frequency (GHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
4.0	0.873	-40.0	1.890	131.0	0.023	67.8	0.887	-17.8
5.0	0.862	-48.9	1.797	120.3	0.025	54.0	0.866	-23.0
6.0	0.794	-55.4	1.658	108.5	0.035	1.8	0.816	-25.8
7.0	0.799	-63.0	1.644	97.8	0.019	-5.8	0.800	-32.4
8.0	0.795	-67.7	1.665	86.7	0.026	-104.1	0.908	-36.6

A single-stage FET amplifier has a dynamic range of +10 to -30 dB gain for a second-gate control voltage variation of 0 to -3.5 V.

*Nippon Electric Company, Japan.

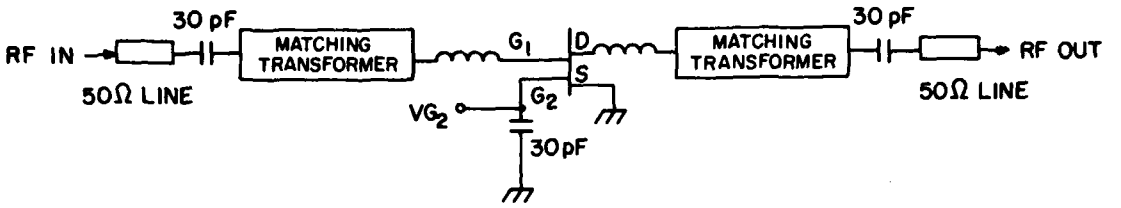


Figure 1. Matching networks for a dual-gate FET amplifier.

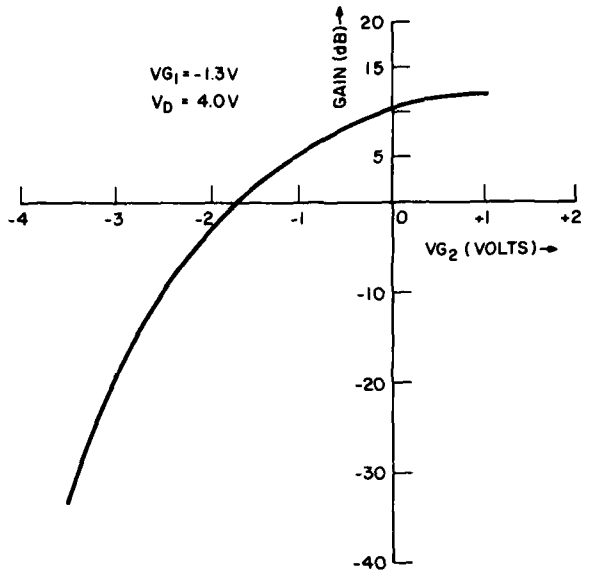


Figure 2. Variation of gain of dual-gate FET amplifier with second-gate bias.

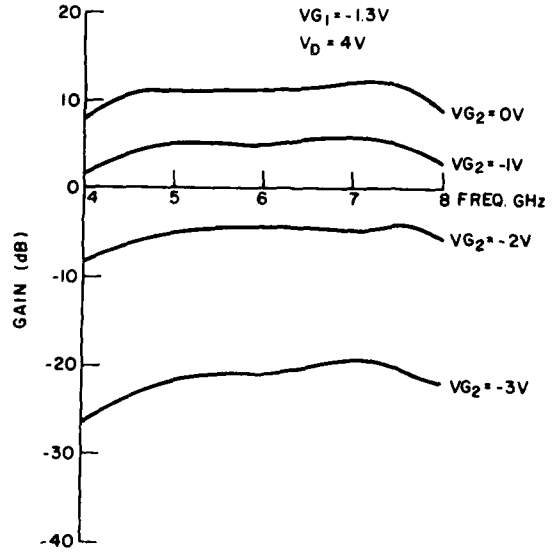


Figure 3. Gain vs VG_2 of dual-gate FET amplifier over 4- to 8-GHz band.

SECTION III

LINEAR AMPLIFIER AND AGC

The design of the linear amplifier with variable gain and constant output power is shown in Fig. 4. It is a five-stage amplifier; the first and the last stage amplifiers do not have built-in AGC. The first stage is intended for providing sampling of input signal, and the last stage is intended for providing external setting of the output power. The middle three stages are advanced AGC control stages. The circuit configuration for one AGC control unit is depicted in Fig. 5. As shown in Fig. 5, the signal at the input of the amplifier is sampled through a 10-dB coupler and is detected and processed at video frequencies to dynamically preadjust the gain of the amplifier.

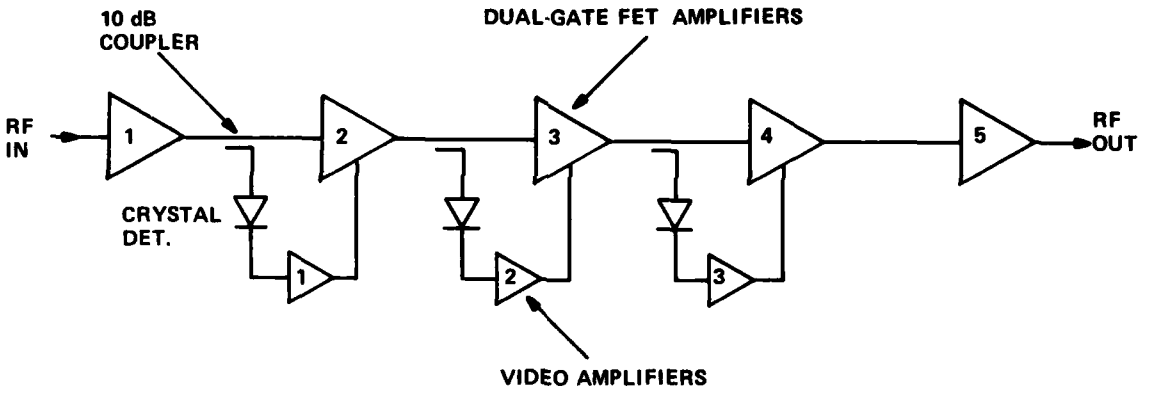


Figure 4. Schematic of variable-gain, constant-output power amplifier.

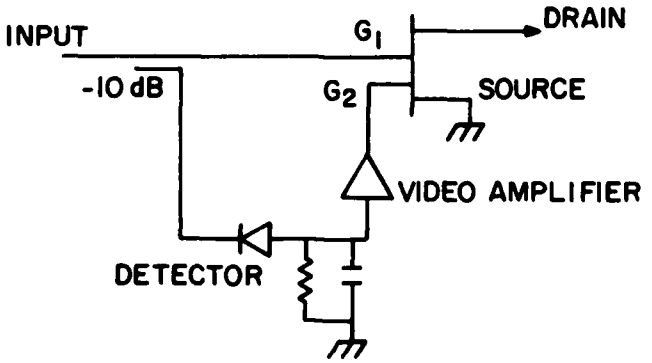


Figure 5. Advanced AGC control.

The video amplifier required in the AGC control unit should have a gain of 40 dB and a bandwidth greater than 350 MHz to provide enough control voltage to the second gate of FET for dynamically controlling the gain and for meeting the response time of 1 ns. A three-stage video amplifier was designed using Motorola rf hybrids MWA 110, MWA 120, and MWA 130 in cascade. The schematic of the amplifier is depicted in Fig. 6, and the characteristics of each rf hybrid amplifier are given in Table 2.

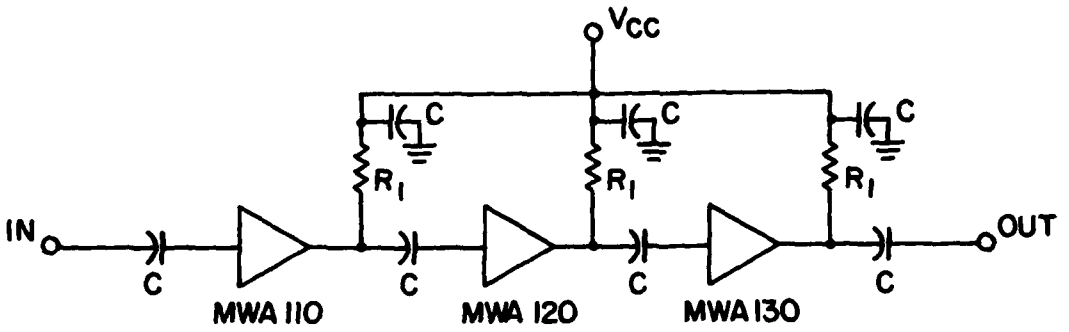


Figure 6. Video amplifier.

TABLE 2. CHARACTERISTICS OF rf HYBRID AMPLIFIERS

rf Hybrid	Frequency Range (MHz)	Gain (dB)	Noise Figure (dB)	Output at 1-dB Compression (dBm)
MWA 110	0.25 - 400	14	4	-2.5
MWA 120	0.25 - 400	14	5.5	+8.2
MWA 130	0.25 - 400	14	7.0	+18

The characteristics of the three-stage video amplifier are:

Bandwidth	:	0.25 to 400 MHz
Gain	:	40 dB
Voltage Output (max)	:	2.5 V

It is important to note in Fig. 4 that there is no isolator used between the different stages of the amplifier. The input and output matching circuits of each dual-gate FET amplifier were designed to match to 50-ohm line impedance. Therefore, the dual-gate FET amplifiers can be directly cascaded to each other.

For the sake of completion and to show the improvement, the design of the linear amplifier of the breadboard model is presented in Fig. 7. The video amplifier (commercially available) used in this circuit had a gain of 25 dB only; therefore, 3-dB couplers were used for sampling the rf power. In addition, a rf amplifier was used in the AGC control unit to provide sufficient voltage to the second gate of the dual-gate FET amplifer.

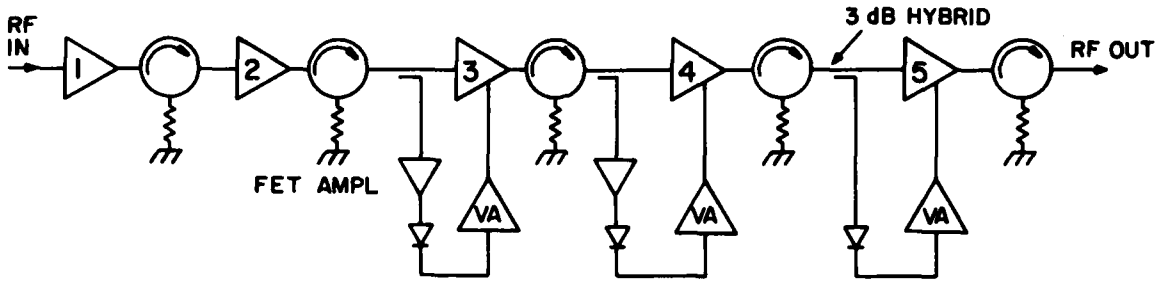


Figure 7. Design of the breadboard amplifier.

SECTION IV

PERFORMANCE AND TEST RESULTS

The overall linear amplifier shown in Fig. 4 was assembled and tested over the 4- to 8-GHz band. A photograph of the amplifier is shown in Fig. 8. The variation of output power of the linear AGC amplifier as a function of frequency for different input-power levels (-45 to 0 dBm) is shown in Fig. 9. The variation of output power is within ±2 dB in the 4.5- to 7.5-GHz (3-GHz band) frequency range for a variation in input-power levels of -45 to 0 dBm.

Figure 10 shows the pulse response of the amplifier. The input pulse at -5 dBM power level is shown in Fig. 10(a); the output rf pulses of the amplifier for different rf inputs are shown in Figs. 10(b), (c), and (d). It is seen that the output power is constant (within its variation) for different input power levels.

The response time of the amplifier was tested for two different input pulses of different amplitude separated by 20 ns. Figure 11 shows the two rf input pulses, both of 0 dBm power level. They are separated by 20 ns, and the pulse width is 300 ns each. Figure 12 shows the output pulses corresponding to the input condition shown in Fig. 11. Figure 13 shows the rf output pulses for two input levels of -10 and -40 dBm. Figure 14 shows the two rf output pulses for two input power levels of -5 and -25 dBm. The results in Figs. 11 through 14 show that the response time of the amplifier is better than 15 ns. This is limited by the measurement system because the rise time of the PIN modulators used for rf pulsing is 15 ns. Furthermore, these results showed that the amplifier can maintain a constant output power under multipulse condition.

We have also carried out an experiment to determine the capability of the amplifier to process the amplitude-modulated pulse. The input pulse was amplitude modulated with a 3-MHz sinusoidal signal. Figure 15 shows the modulated rf input pulse, and Fig. 16 shows the rf output pulse. The amplifier successfully retained the modulation envelope as shown in Fig. 16.

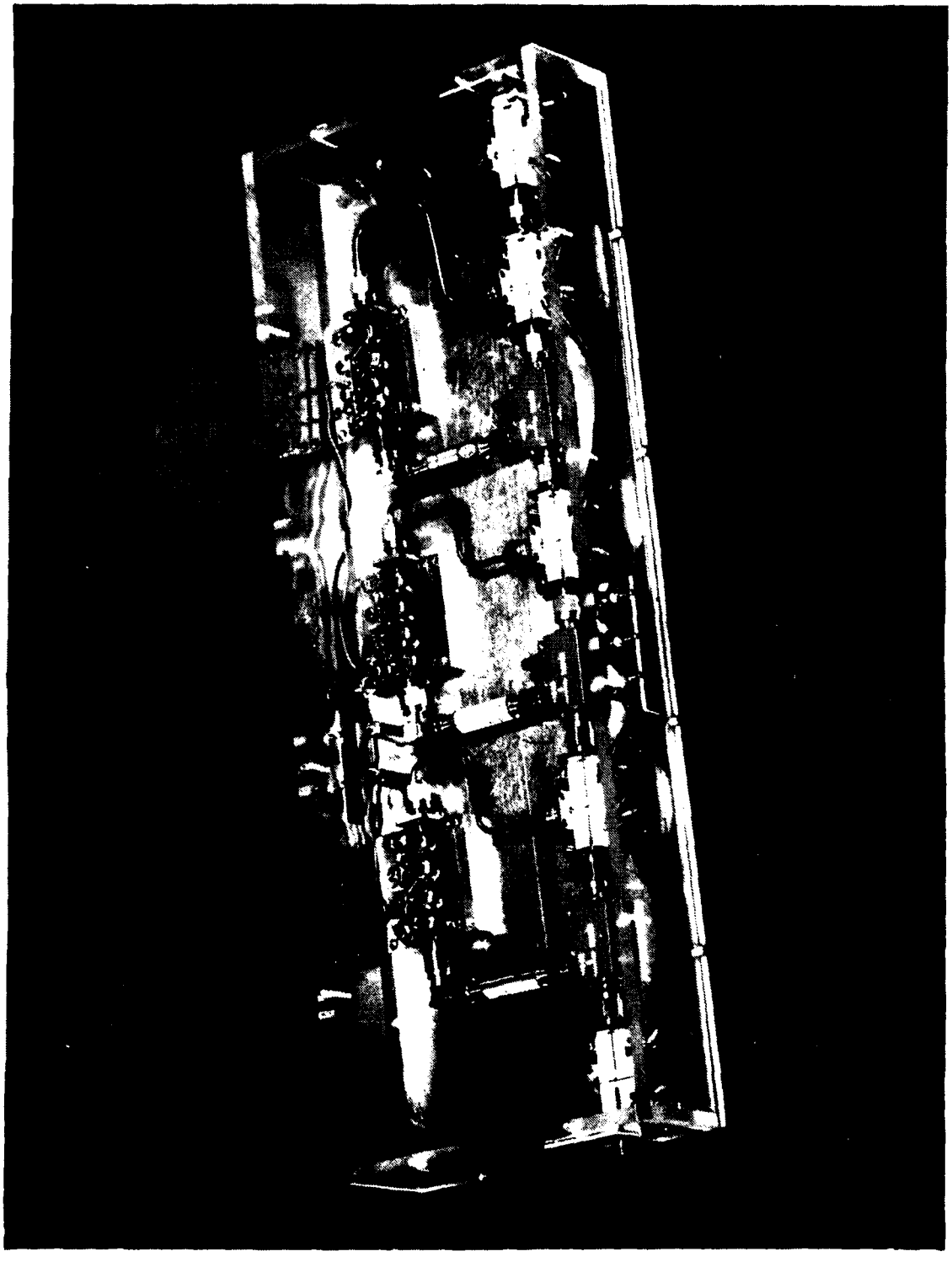


Figure 8. Photograph of the amplifier.

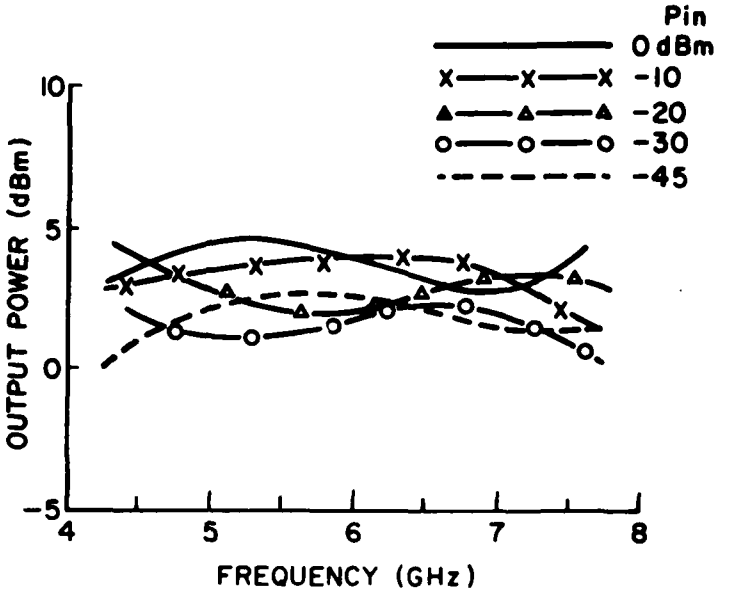
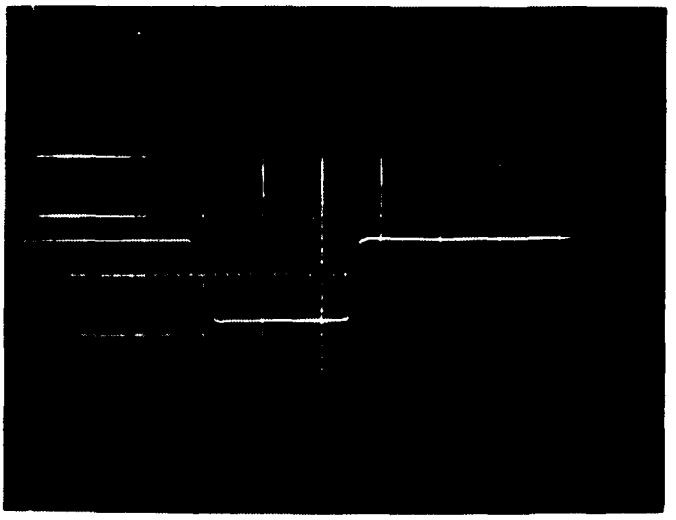


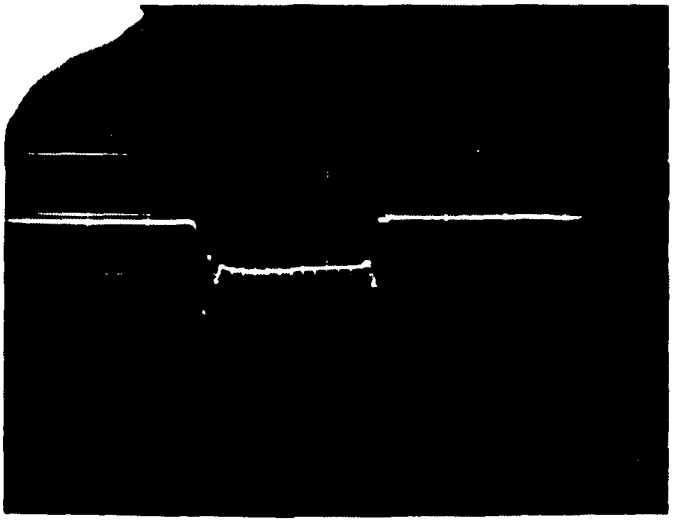
Figure 9. Variation of output power with frequency for different input power levels.



Scale: Vertical: 0.05 V/div
Horizontal: 100 ns/div

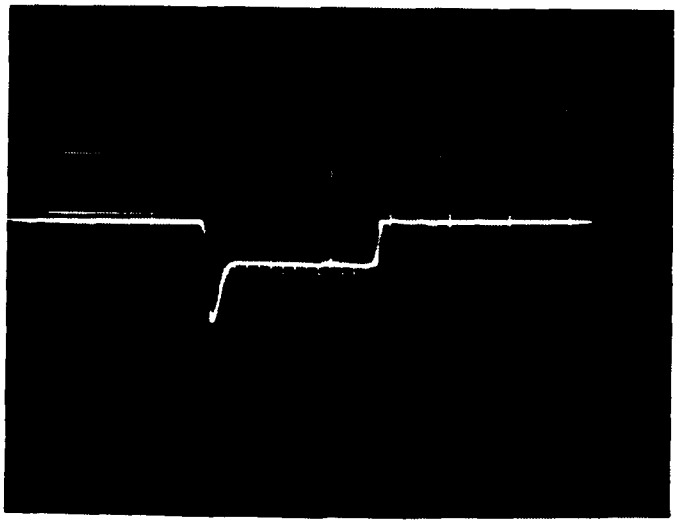
(a) rf Input pulse (P_{in} = -5 dBm)

Figure 10. Pulse response of the amplifer.



Scale: Vertical: 0.14 V/div
Horizontal: 100 ns/div

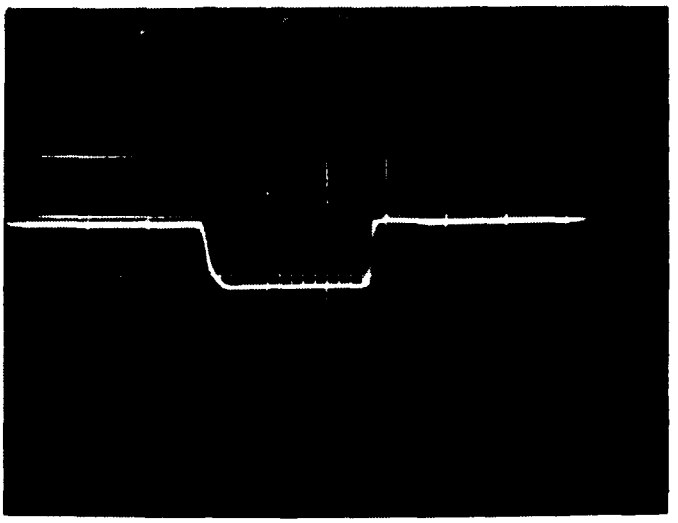
(b) rf Output pulse (P_{in} = 0 dBm)



Scale: Vertical: 0.1 V/div
Horizontal: 100 ns/div

(c) rf Output pulse (P_{in} = 20 dBm)

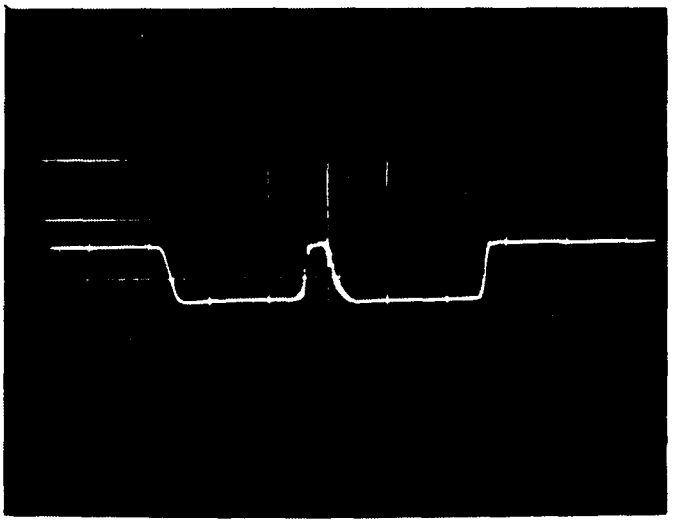
Figure 10. (Continued)



Scale: Vertical: 0.1 V/div
Horizontal: 100 ns/div

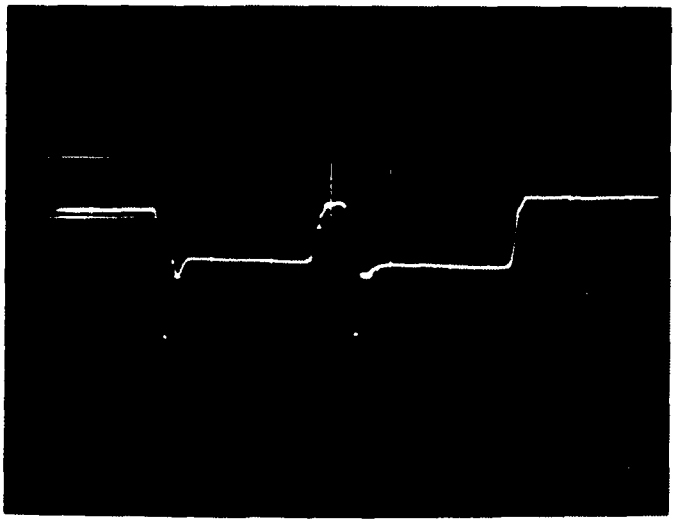
(d) rf Output pulse (P_{in} = -40 dBm)

Figure 10. (Continued)



Scale: Vertical: 0.05 V/div
Horizontal: 100 ns/div

Figure 11. rf Input pulses (0 dBm).



Scale: Vertical: 0.1 V/div
Horizontal: 100 ns/div

Figure 12. rf Output pulses. Input power for first and second pulses = 0 dBm.

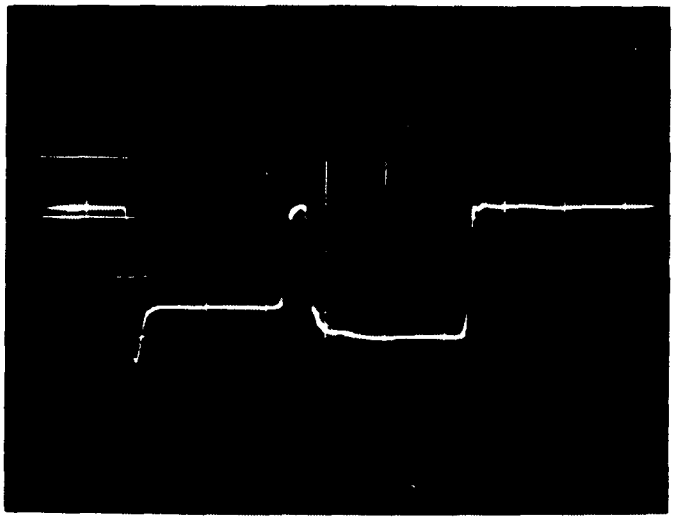


Figure 13. rf Output pulses. Input power, first pulse = -10 dBm; second pulse = -40 dBm.

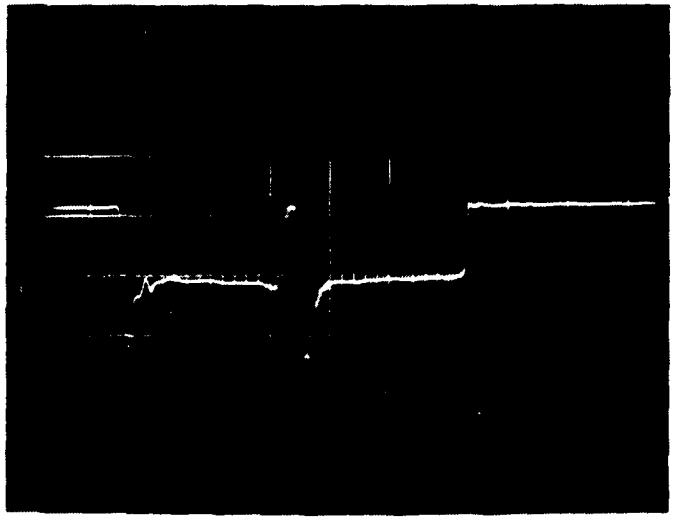


Figure 14. rf Output pulses. Input power, first pulse = -5 dBm; second pulse = -25 dBm.

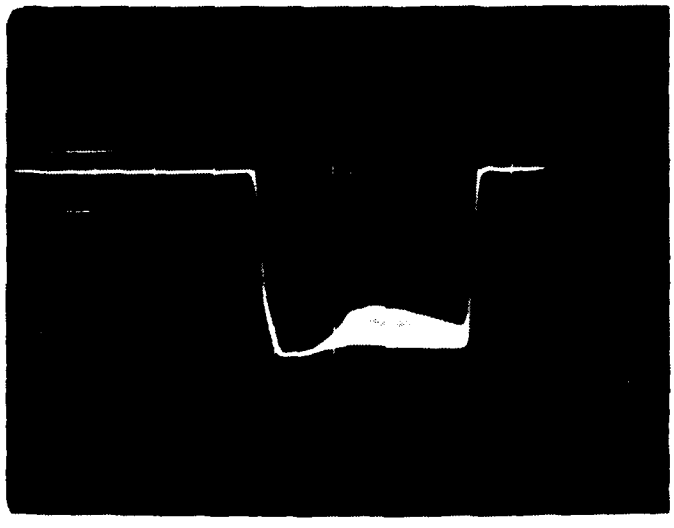


Figure 15. Amplitude-modulated input rf pulse.

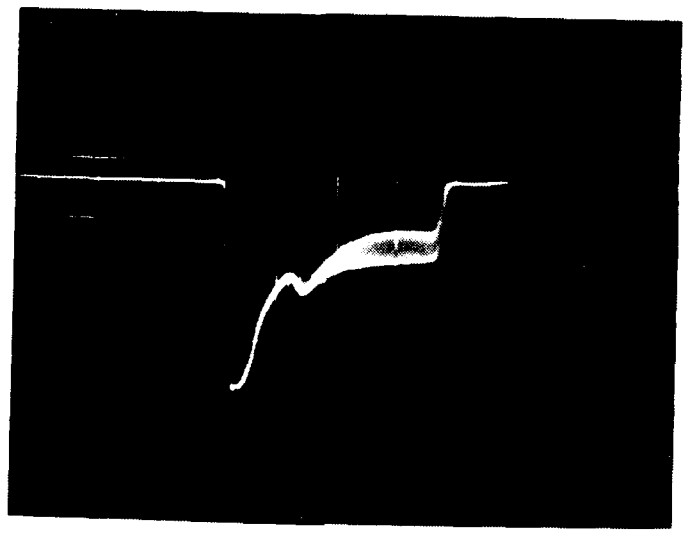


Figure 16. Amplitude-modulated output rf pulse.

SECTION V

CONCLUSIONS

The program has been completed successfully with the delivery of a breadboard model and an improved linear AGC amplifier that features constant output power over its entire dynamic range. The amplifier has a bandwidth of 4.5 to 7.5 GHz (3 GHz). It delivers a constant output power of 3 ±2 dBm over its dynamic range of -45 to 0 dBm of input power. The response time of the amplifier is better than 15 ns.

The linear AGC amplifier developed under this program has the following key features. (1) It preserves amplitude modulation of the incoming signal. (2) It can perform normal AGC function under a multiple-pulse condition. This characteristic may prove to be very useful for handling multiple threats. (3) It is very versatile. It can provide separate ports to facilitate output power level adjustment and input signal detection and monitoring. (4) It has fast response. The rise time and fall time of this amplifier are better than 15 ns which is limited by the measurement system.

APPENDICES

APPENDIX A

A 4–8 GHz DUAL GATE M.E.S.F.E.T. AMPLIFIER

Indexing term: Microwave amplifiers

A two-stage dual-gate f.e.t. amplifier with small signal gain of 20 ± 0·75 dB, covering an octave bandwidth (4–8 GHz) and having a dynamic gain control range in excess of 60 dB is reported. The gain frequency response, input and output v.s.w.r. are described as a function of second-gate voltage. The performance of the dual-gate f.e.t. amplifier as a fast r.f. switch is also presented.

This letter describes the results obtained on a 2-stage dual-gate f.e.t. linear amplifier designed to cover the 4–8 GHz band. The advantage of using a dual-gate f.e.t. as a broadband amplifier compared to a single gate f.e.t. is the availability of the second gate for additional signal processing. This characteristic makes the dual-gate amplifier inherently suitable for many e.w. and e.c.m. applications.

The dual-gate f.e.t.s used in this amplifier were characterised as a three-port network. Using a computer program developed for this purpose, the second-gate termination was optimised to yield maximum available gain from the device. The matching networks were then designed for G1 and the drain to realise the maximum gain from the amplifier at a given bias. The picture of the complete amplifier and the schematic of a single stage are shown in Fig. 1.

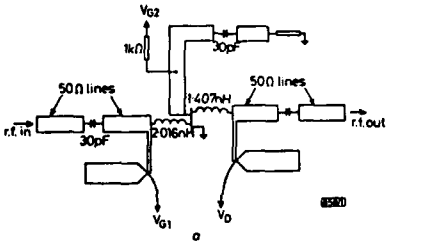


Fig. 1 *Amplifier*
a Schematic of single stage
b Photograph of the amplifier

The gain of the amplifier for various levels of second gate voltage with constant r.f. drive is shown in Fig. 2*a*. As shown, the amplifier has a maximum gain of 20 dB with V_{G2} at +1·0 V. The gain flatness is essentially maintained with different bias voltages applied to the second gate down to an insertion loss of 40 dB with the second gate at −2·0 V. The same results are plotted in Fig. 2*b* as a function of the second-gate bias to emphasise the inherent gain control capability of the dual-gate amplifier.

Fig. 3*a* shows a typical plot of output power against input power at mid-band. The amplifier provided 20 mW at the 1 dB gain compression point. The output power does not change considerably when the amplifier is driven beyond the

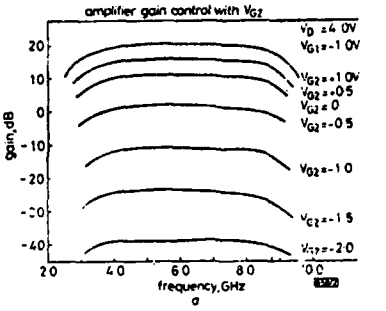


Fig. 2 *Gain against V_{G2}*
a Constant r.f. drive
b At 6 GHz, $V_D = 4V$, $V_{G1} = -1V$

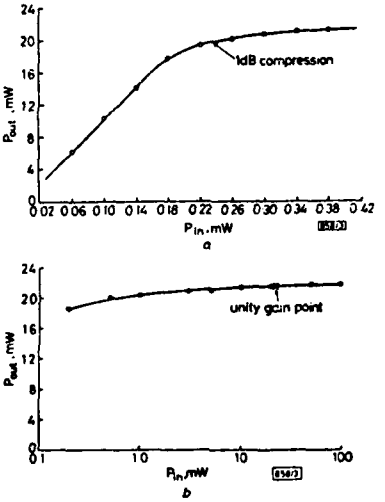


Fig. 3 *P_{in} against P_{out}*
a $V_D = 4V$, $V_{G1} = -1V$, $V_{G2} = 1V$
b Overdrive characteristics of the amplifier

Reprinted from ELECTRONICS LETTERS 16th March 1978 Vol.14 No.6 pp. 167–168

onset of saturation. As shown in Fig. 3b, this amplifier, when operating in the limiter mode, had a compression slope (given by $\Delta P_{in}/\Delta P_{out}$) of 25 dB, around drive levels of unity gain and beyond. This level of power compression indicates its power limiting capability.

An important feature of this amplifier is the relative invariance of its input/output v.s.w.r. as a function of the second-gate voltage. Varying the second-gate voltage to change the gain of the amplifier, over the 60 dB dynamic control range, has very little effect on the 1·8:1 input and 2:1 output v.s.w.r., originally obtained at full gain. The results are plotted in Fig. 4. This characteristic is very important in ensuring that good fine-grain gain is maintained and no gain perturbations occur over the 4 GHz bandwidth, independent of the second gate voltage.

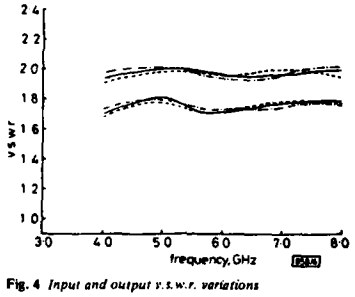


Fig. 4 *Input and output v.s.w.r. variations*

$V_D = 4V, V_{G1} = -1V$
—— $V_{G2} = 1V$
– – – $V_{G2} = 0V$
– · – $V_{G2} = 2V$

With r.f. input applied to the first gate, the second gate can be used for high speed video switching or amplitude modulation. Fig. 5 illustrates the amplifier response to a square wave, applied to the second gate. The input pulse had a rise and fall time of 200 ps and pulse duration of 1·5 ns (as shown in the upper half of the picture). This pulse drives the second gate of the amplifier from 0 to −0·7 V, thus changing the gain of the amplifier by about 18 dB while causing less than 100 ps increase in rise and fall times. The inherently fast switching or gain control makes dual-gate f.e.t.s very useful for ultra fast a.g.c. and anti-jamming control circuitry for e.w. applications.

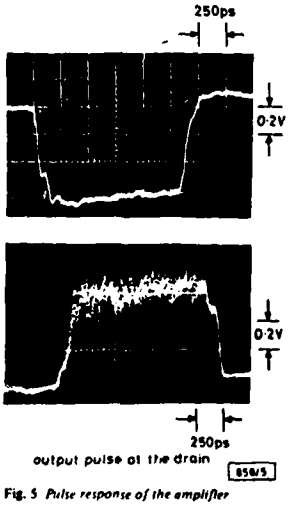


Fig. 5 *Pulse response of the amplifier*

Phase shift versus frequency was very linear over the complete operating band, as shown in Fig. 6. Group delay (deviation of phase shift with respect to radian frequency) was calculated to be 0·3 ns.

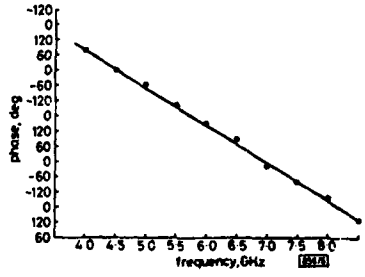


Fig. 6 *Phase shift against frequency*

Conclusion: In conclusion, the dual-gate f.e.t. appears to offer important advantages in the processing of wideband microwave signals. Fast switching, a.g.c. and limiting are examples of these new capabilities. Improved isolation of the broadband gain mechanism from the signal manipulation characteristics is afforded by the control applied by the second gate.

Acknowledgments: This work was completed with the interest and talents of many people. In particular, we would like to thank H. Huang for his encouragement, J. Brown and M. Kunz in the diligent circuit assembly work. B. Dornan's help in making the measurements and J. B. Klatskin's help in programming are also greatly appreciated.

JITENDRA GOEL
HERBERT J. WOLKSTEIN
RCA Laboratories
Microwave Technology Center
David Sarnoff Research Center
Princeton, New Jersey 08540, USA

19th January 1978

References

1 LIECHTI, C. A.: 'Performance of dual-gate m.e.s.f.e.t.s as gain controlled low noise amplifiers', *Proceedings of the 1975 IEEE international solid state circuits conference*, Phila., PA
2 ROSEN, A., WOLKSTEIN, H., GOEL, J., and MATARESE, R. J.: 'A dual-gate GaAs f.e.t. r.f. power limiter', *RCA Review*, June 1977

0013-5194/78/0858-0167 $1.50/0

APPENDIX B

A Dual-Gate GaAs FET RF Power Limiter*

A. Rosen, H. J. Wolkstein, J. Goel, and R. J. Matarese

RCA Laboratories, Princeton, N.J. 08540

Abstract–This report describes a preliminary investigation of a novel rf power limiter-amplifier that makes use of a recently developed dual-gate GaAs FET stage with a small-signal gain of 7 dB and a compressive gain slope (when overdriven) of 14.8 dB at the unity gain point. When operated in the power-limiting mode, several cascaded stages of this amplifier can be used to drive a companion FET discriminator to provide unambiguous frequency-to-voltage conversion.

FET Dual-Gate RF Power Limiter

A conventional means of achieving constant output power independent of drive variation or frequency is to utilize a multistage high-gain amplifier chain. The output stages of this amplifier operate in saturation regions where the output-power variations are greatly compressed, even for large variations in the input-power range. This mode of operation is depicted for several stages in Fig. 1.

For use with a frequency discriminator, for example, to obtain a frequency accuracy of 1 MHz in a 4-GHz bandwidth, the rf-limiter output must be flat to within 0.025%. This is equivalent to an incremental power output fluctuation of 1 part in 4000, 36 dB down from saturation over the total variation in input drive range. Assuming an input drive range of 31 dB, the combined value of input power swing and output limiting

* RCA Acknowledges the support of the Naval Electronic Systems Command, under Contract No. N00039-76-C-0-0280, in the initial work associated with the FET limiter.

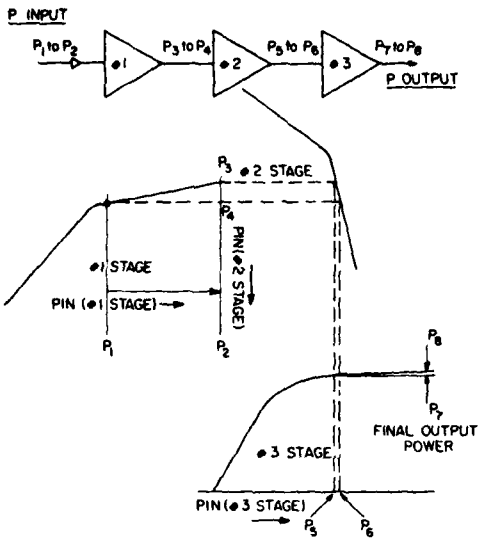


Fig. 1—A cross plot of power-input compression for a three-stage overdriven amplifier.

is equivalent to an overall compression ration of 67 dB ($1250/2.50 \times 10^{-4} = 5 \times 10^6$).

A dual-gate GaAs FET amplifier stage[1] has recently been tested in C-band with adjustments made in the operating voltage parameters to emphasize its capability to achieve rf power limiting. The resulting curve is shown in Fig. 2.[2] Using the test setup shown in Fig. 3, the rf power output of the stage, which has a small signal gain of ~ 7 dB, was driven

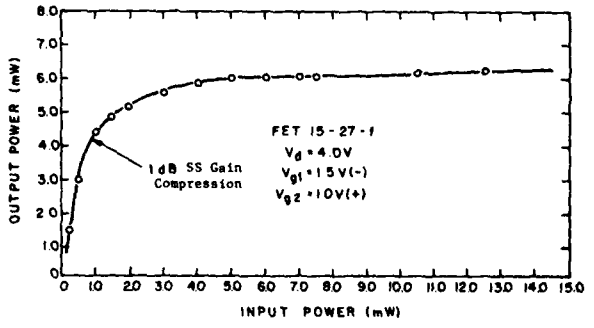


Fig. 2.—Limiting characteristics of dual-gate GaAs FET (operated at 5 GHz).

over the 0 to +15-mW input power drive range. Under these operating conditions, the stage goes to unity gain at an input drive level of 6 mW. At this approximate drive level and beyond, the compressive slope of the limiter (given by $\Delta P_{in}/\Delta P_{out}$) is 9 mW/0.3 mW or 14.8 dB. This level of power compression or limiting per stage provides an excellent capability on which to base an FET limiter–amplifier design.

The use of a dual-gate amplifier provides important functional advantages over the single-gate FET because of its flexibility.[3–5] One of the gates (G2) is adjusted to ensure proper gain level and saturation

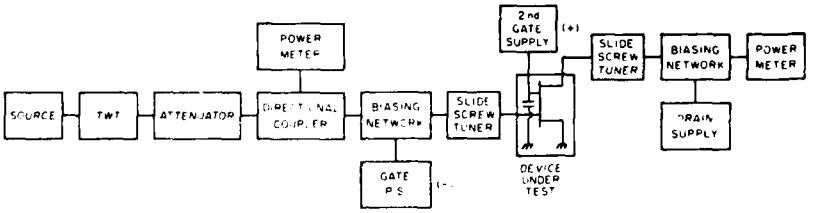


Fig. 3—Measurement setup for dual-gate FET.

operation, while the input rf signal is connected to the additional gate (G1). The dual-gate device greatly reduces the capacitance between the signal input gate and the drain electrode. This reduced capacitance provides for increased small-signal gain per stage when compared to equivalent single-gate devices with the same gate length. The dual gate also substantially reduces direct rf feedthrough from input to output; which is important in an overdrive amplifier.

Measurements were also performed to evaluate the limiting properties of the single-gate high-power FET devices of the type discussed previously by I. Drukier et al.[6] We found that the saturation characteristic of those devices was inferior to that obtained using a dual-gate FET device, and therefore a greater number of stages was required to obtain the same compression ratio.

In conclusion, we have demonstrated the use of a dual-gate FET as a limiter. Used at 5 GHz, the device has a small signal gain of 7 dB and has demonstrated a compression ratio ($\Delta P_{in}/\Delta P_{out}$) of 14.8 dB. This level of limiting per stage provides an excellent basis for the design of an FET limiter–amplifier chain. The number of stages, operating parameters, and power levels may be adjusted to fit particular operational requirements. Such a limiter, operated, for example, with an FET discriminator such as the one described in Ref. [7], represents an attractive approach for an EW receiver.

Acknowledgments

The authors wish to thank D. Mawhinney and L. Napoli for many helpful discussions and suggestions and E. Mykietyn for diligent circuit assembly and device testing.

References:

[1] R. H. Dean and R. J. Matarese, "Submicrometer Self-Aligned Dual-Gate GaAs FET," *IEEE Trans. on Electron Devices*, p. 358, June 1975.

[2] A. Rosen and D. D. Mawhinney, "FET Frequency Discriminator," Final Report, NESC Contract No. N00039-76-C-0280, Feb. 1977.

[3] Charles A. Liechti, "Performance of Dual-Gate GaAs MESFETs as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," 1975 IEEE International Solid-State Circuits Conf., Phila., Pa.

[4] S. Asai, F. Mural, and H. Kodera, "The GaAs Dual-Gate FET with Low Noise and Wide Dynamic Range at Microwave Frequencies," Int. Electron Devices Conf. Digest of Technical Papers, p. 64 (1973).

[5] M. Maeda and Y. Minai, "Application of Dual-Gate GaAs FET to Microwave Variable-Gain Amplifier," Int. Microwave Symposium Digest of Technical Papers, p. 351 (1974).

[6] I. Drukier et al, "Medium Power GaAs Field-Effect Transistors," *Electronics Lett.*, **11**, No. 5, p. 104, March 1975.

[7] A. Rosen, D. Mawhinney, and L. S. Napoli, "A Novel FET Frequency Discriminator," *RCA Review*, **38**, p. 238, June 1977 (this issue).

APPENDIX C

United States Patent [19]

Wolkstein et al.

[11] **4,167,681**

[45] **Sep. 11, 1979**

[54] **MICROWAVE POWER LIMITER COMPRISING A DUAL-GATE FET**

[75] Inventors: **Herbert J. Wolkstein**, Livingston; **Arye Rosen**, Cherry Hill; **Jitendra Goel**, Kendall Park, all of N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **838,720**

[22] Filed: **Oct. 3, 1977**

[51] **Int. Cl.**[2] **H03G 11/04; H04B 3/04**

[52] **U.S. Cl.** ..... 307/237; 307/264; 328/171; 328/172; 333/17 L

[58] **Field of Search** ..... 307/237, 264; 333/17 L; 328/169-172

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,079,325 3/1978 Mawhinney et al. ..... 307/233 R X

OTHER PUBLICATIONS

Rosen et al., *RCA Review* (pub.), vol. 38, 6/1977; pp. 253-256.

Int'l Microwave Symposium; *Microwaves* (pub.), pp. 9-10; 6/77.

Fukuda et al., IEEE Microwave Theory and Techniques (MTT) Conf.; 6/1977.

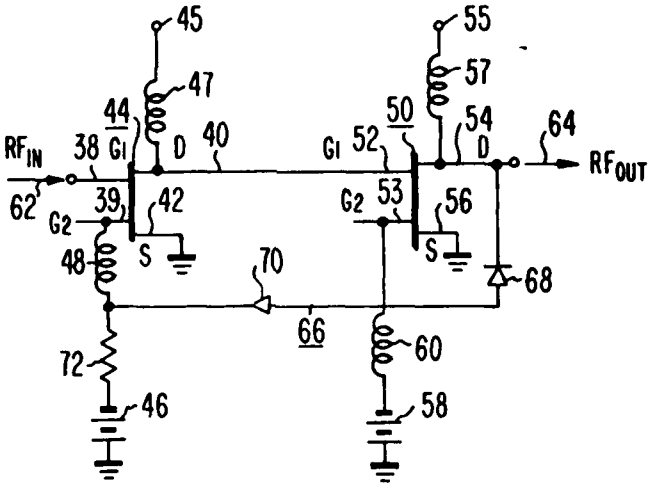
Primary Examiner—Larry N. Anagnos

Attorney, Agent, or Firm—H. Christoffersen; Joseph D. Lazar

[57] **ABSTRACT**

A microwave power limiter for generating an output RF signal of substantially constant power level in response to an input RF signal of varying power level comprises a dual gate field effect transistor (FET). The FET is biased such that the RF power output variation is small compared to the input power variation in the saturation region. A number of FET cascaded stages may be utilized to reduce this power output variation. A small signal amplifier including a number of FET cascaded stages may be employed in the limiter to increase the power level to that gain or drive level compatible with the saturated FET stages.

5 Claims, 9 Drawing Figures



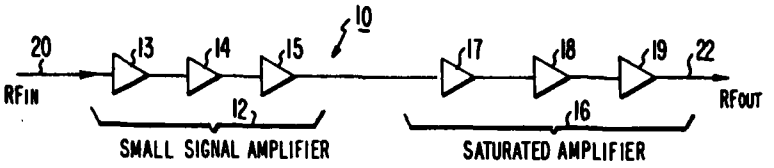


Fig. 1

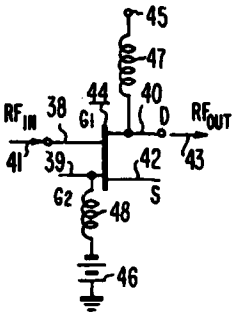


Fig. 4a

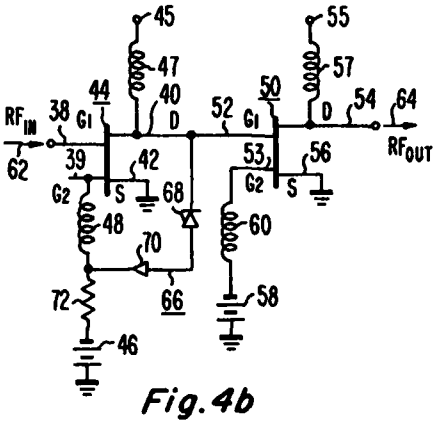


Fig. 4b

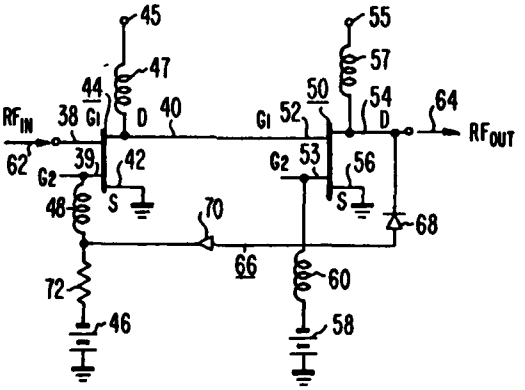


Fig. 4c

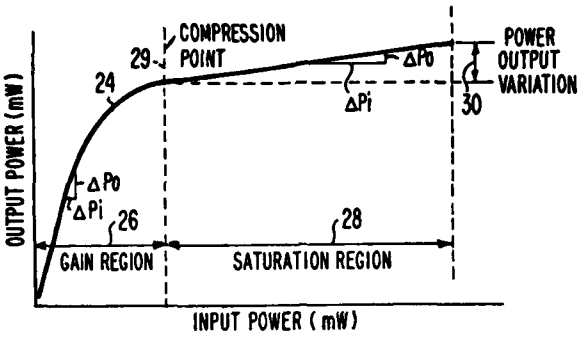


Fig. 2

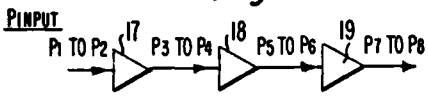
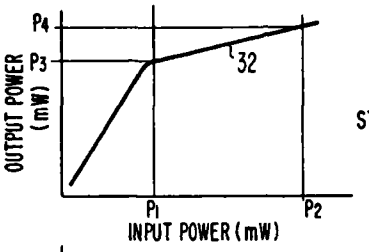
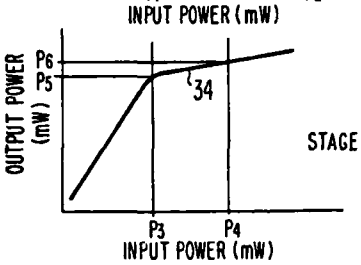


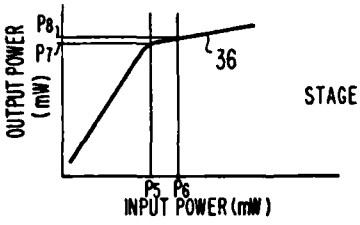
Fig. 3a



STAGE 17 Fig. 3b



STAGE 18 Fig. 3c



STAGE 19 Fig. 3d

MICROWAVE POWER LIMITER COMPRISING A DUAL-GATE FET

The Government has rights in this invention pursuant to Contract No. N00039-76-C-0280 awarded by the Department of the Navy.

CROSS REFERENCE TO RELATED APPLICATIONS

Of interest is the following copending U.S. application Ser. No. 838,656, filed on Oct. 3, 1978, entitled "Microwave Power Limiter Comprising a Single-Gate FET," based on the invention of Daniel David Mawhinney, Herbert J. Wolkstein, Arye Rosen and Zygmond Turski and assigned to the same assignee as is the present invention.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a microwave power limiter and, more particularly, to a power limiter including a dual gate field effect transistor.

2. Description of the Prior Art

Many commercial and military systems require a source of constant RF power while simultaneously tolerating a wide variation of RF input power to the same system. It is often a system requirement that this fixed output power level be obtained over a wide frequency bandwidth. Such a power limiter having these desirable characteristics may be used as an RF amplifier, front end receiver where fixed output power is necessary for radar terrain mapping and associated video osscilloscope displays. Other limiter applications include receivers that are used for phase and frequency identification for electronic countermeasure (ECM) systems. In this application, fixed input power is generally applied to phase discrimination for accurate conversion of frequency (or phase) into an output dc voltage. A limiter having these properties may also be utilized for bi-phase and digital communications systems where coded binary signals are received and cannot be reconstructed to constant power output levels independent of the amplitude variations of the receiving antenna.

One of the conventional approaches for achieving constant (or standardized) output power, independent of drive variation and frequency, is to utilize a multistage high gain amplifier chain. This amplifier chain is designed to constrain operation of several of the output stages to the overdriven or saturation region where the output power swing is greatly compressed in spite of large variations in the input power range to the chain. Both bipolar silicon transistors and tunnel diode amplifiers (TDA) are used in such multistage limiters. The bipolar transistor limiter is restricted, however, to low frequency applications and is not often selected for use. For other limiting amplifier circuits see U.S. Pat. No. 3,940,704 issued Feb. 24, 1976 and U.S. Pat. No. 3,999,084 issued Dec. 21, 1976 which use operational amplifiers and U.S. Pat. No. 3,932,768 issued Jan. 13, 1976 and U.S. Pat. No. 4,008,440 issued Feb. 15, 1977 which utilize differential amplifiers.

The TDA is in wide use and has heretofore provided desirable amplifier-limiter capabilities. The TDA limiter suffers, however, from diverse problems and disadvantages, limiting the applications and performance of the TDA limiter. For instance, the power output for a broadband TDA is limited to levels of about −6 dbm (0.25 mW) or less. This power output level produces an RMS output voltage of less than 0.1 volt, with a video detector circuit having an impedance of 100 ohms. Such output is too low to drive a conventional phase interferometer-discriminator and detector without the use of video amplifiers. Another disadvantage of the TDA is that since it is a two terminal device used as a reflection amplifier, circulators for each stage and isolators between every other stage are needed for stability of the limiter. Such a multiplicity of interconnected components typically using ferrite materials produces many reflections which add in-and-out-of-phase resulting in considerable fine and coarse grain structure which directly reduces the accuracy when used with a discriminator. In such a discriminator system, for example, a variation of about 0.1 db will case an attendant error of approximately 80 MHz in a 4GHz band system. Furthermore, the use of necessary circulators and isolators in a multistage TDA configuration requires extensive circuitry and thereby, a relatively costly device.

For microwave discriminator applications, the output power variation as the input to the discriminator circuit is to be minimal. For example, to approach a frequency accuracy of 1 MHz in a 4 GHz bandwidth, due to output power variations of the RF limited output wave, would require an output power deviation or flatness of 0.025%. This is equivalent to an incremental power output fluctuation 36 db from saturation over the total variation in input drive range. With an input drive range of, for instance, 30 db, the combined values of input power swing and output limiting is equivalent to an overall compression ratio of 66 db. Considering the capabilities and costs, such a performance would be difficult, if not impossible, to achieve with the TDA limiter.

Use of Gallium Arsenide (GaAs) single gate field effect transistors (FET) arranged in a multistage configuration and operated in a satured condition has been suggested. (See the article in *Microwaves*, entitled "GaAs FETs Gain Ground in Oscillators, Mixers and Limiters," June, 1977, pages 9-10, and a paper published in the minutes of the IEEE Microwave Theory and Techniques (MTT) conference in San Diego, June, 1977, entitled "A New Microwave Amplitude Limiter Using GaAs Field Effect Transistor," by S. Fukuda, M. Kitamura, Y. Ara and I. Haga.) The single gate FET has a relatively high parasitic capacitance and results in an undesirably high feedback capacitance between the gate and drain electrodes. This feedback capacitance tends to reduce the small signal gain of the amplifier. The RF feedthrough from input to output of the FET is also decreased by this capacitance resulting in reduced saturation properties. These deficiencies can often be overcome by increasing the number of FET stages in the limiter disadvantageously adding, however, to the cost as well as size of the device.

SUMMARY OF THE INVENTION

According to the present invention, a power limiter generates an output RF signal of substantially constant power level in response to an input RF signal of varying power level. The limiter comprises a field effect type transistor having first and second gate, drain and source electrodes, the first gate electrode being receptive of the input RF signal. Included in the limiter is means for biasing the second gate electrode of the transistor such that the transistor operates in a gain region character-

ized by a power curve having a slope whose change in output power is substantially equal to or greater than the change in input power. The transistor also operates in a saturation region characterized by a power curve having a compression slope whose change in output power is substantially less than the change in input power such that the final output power variation is small compared to the input power variation. The substantially constant RF signal is generated over the saturation region.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a diagrammatic representation of one embodiment of the invention showing a number of amplifier stages in cascaded arrangement.

FIG. 2 is a graph showing the output power versus the input power of the power limiter of the present invention.

FIG. 3(*a*) is a block diagram illustrating the cascaded arrangement and the power distribution between the stages of the saturated amplifier of the preferred embodiment of the present invention.

FIGS. 3(*b*) to 3(*d*) are curves graphically showing the power variation of the cascaded stages of FIG. 3(*a*).

FIGS. 4(*a*) to 4(*c*) are schematic representations of biasing arrangements utilized to bias the FETs of the amplifier stages in the limiter of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to the drawing, there is shown in FIG. 1, a microwave power limiter 10, comprising a multistage small signal amplifier 12 and a multistage saturated amplifier 16. Amplifiers 12 and 16 each comprise three stages 13, 14 and 15 and 17, 18 and 19, respectively, for purposes of illustration although any number of stages depending upon the desired operational characteristics of limiter 10 may be utilized. Stages 13, 14 and 15 of amplifier 12 and stages 17, 18 and 19 of amplifier 16 are connected in cascaded arrangement and each stage includes a dual-gate field effect transistor (FET) as will be explained in detail. An input RF signal 20 of varying power level is received by amplifier 12. An output RF signal 22 of constant power level is generated by limiter 10 in accordance with the invention as the output of amplifier 16. The stages of amplifiers 12 and 16 are biased by suitable bias arrangements (not shown in FIG. 1), the biasing of the stages to be described more fully with respect to FIGS. 4*a*-4*c*.

As shown in FIG. 2, the FETs of the stages of amplifiers 12 and 16 are biased to operate to have their output power vary as a function of input power in accordance with curve 24. FET characteristic power curve 24 has a gain region 26 and a saturation region 28. In gain region 26 the slope of curve 24 is such that the change in output power (ΔPo) is equal to or greater than the change in input power (ΔPi). In the saturation region 28 the slope of curve 24 is such that the change in output power (ΔPo) is substantially less than the change in input power (ΔPi). Over the saturation range 28, the output power of the FET is constant within a power output variation 30. As with conventional amplifiers operating in the saturated condition for limiter applications, the slope of curve 24 in the saturated region 28 is commonly referred to as the "compressive slope" or the power compression ratio of the limiter. As known in the limiter art, the compressive slope is expressed as the input power drive variation versus the output power change, or $\Delta Pi/\Delta Po$.

For power limiter applications, it is desirable to reduce the power output variation 30 to a minimum. The change in output power for an ideal power limiter is zero for changes in input power. Practical factors, such as bias voltages, FET configuration, FET circuitry and the FET material properties, typically limit the achievement of an ideal limiter, generally resulting in a certain amount of power output variation (30) in an individual limiter stage. Cascading of a number of FET stages and operating the FET stages in a saturated or overdriven condition will reduce the final output variation 30 to a level less than that variation for a single stage. By referring to FIGS. 3(*a*) to 3(*d*), such a cascaded arrangement may be more fully understood.

In the cascaded arrangement of FIG. 3(*a*), stages 17, 18 and 19 of saturated amplifier 16 are connected such that output power range (P_3 to P_4) of stage 17 is the input power range to stage 18, and the output power range (P_5 to P_6) of stage 18 is the input power range to stage 19. Power range P_3 to P_4 and range P_5 to P_6 are the output power variations of stages 17 and 18, respectively. P_1 to P_2 is the input power range to stage 17 as received from the output of small signal amplifier 12. P_7 to P_8 is the final power output variation as the output signal of stage 19. Curves 32, 34 and 36 represent the characteristic curves of the FETs of stages 17, 18 and 19 respectively as shown in FIGS. 3(*b*), 3(*c*) and 3(*d*). By applying the output of a preceding stage as the input of a succeeding stage as the FETs are operated in a saturated condition in which the change in output power is less than the change in input power, the final power output variation, e.g., P_7 to P_8, can be reduced, as shown graphically in FIGS. 3(*b*) through 3(*d*). In such a cascaded arrangement the final power output variation can be reduced even further by adding more stages. It should be appreciated that depending upon the power output variation tolerable in a particular limiter operation, cascaded FET stages may not be needed, the output of a single stage being satisfactory.

In the preferred embodiment shown in FIG. 1, small signal amplifier 12 is utilized to produce a power level which is compatible with the desired power level of saturated amplifier 16. The FETs of each of the stages 13, 14 and 15 are biased to operate in the gain region 26 as shown in FIG. 2 such that the change in output power is equal to or greater than the change in input power. By cascading stages operating in the gain region such that the output of a preceding stage provides the input of a succeeding stage the gain level of the final output stage 15 can be increased over the gain level to the input stage 13. It should be understood that the gain level provided by small signal amplifier 12 to saturated amplifier 16 can be changed by increasing or decreasing the number of stages. It should also be appreciated that small signal amplifier 12 may be eliminated in a system where the gain level of the RF input signal 20 is compatible with the gain level of the saturated amplifier 16.

Each of the FETs in the stages of amplifiers 12 and 16 have first gate 38, second gate 39, drain 40 and source 42 electrodes as shown schematically on FET 44 in FIG. 4(*a*). In the preferred embodiment, FET 44 is a Gallium Arsenide (GaAs) metal semiconductor field effect transistor (MESFET), although other field effect type transistors such as, for example, junction field effect transistors (JFET), wherein the current is controlled by an electric field, may also be used. FET 44

may be biased by applying a dc voltage to second gate electrode 39 as by battery 46 through an inductor 48. The other terminal of battery 46 may be grounded. Biasing of FET 44 may also be achieved by pulsed voltages as well as by dc voltages. An input RF signal 41 is received at first gate electrode 38 and an output RF signal 43 is generated at drain electrode 40. Drain electrode 40 is biased by applying a suitable voltage to terminal 45 through an inductor 47, for example.

A biasing arrangement for cascaded FETs is shown in FIG. 4(*b*). For example, FET 44 with the biasing circuit as shown in FIG. 4(*a*), may be cascaded with an FET 50 of a succeeding stage. FET 50 has first gate 52, second gate 53, drain 54 and source 56 electrodes. Drain electrode 40 of FET 44 is connected to first gate electrode 52 of FET 50 and the source electrodes 42 and 56 respectively of each FET 44 and 50 are grounded. A battery 58 provides a predetermined dc voltage to second gate electrode 53 through an inductor 60, the other terminal of battery 58 being grounded. The drain electrode 54 is biased by applying a suitable voltage to terminal 55 through inductor 57, for example. An input RF signal 62 may be applied at first gate electrode 38 and an output RF signal 64 generated at drain electrode 54. In the preferred embodiment of the invention, a feedback network 66 may be connected between the drain electrode 40 and second gate electrode 39 of each of the FETs utilized. Feedback circuit 66 feeds a portion of the output signal from drain electrode 40 back as an input signal to second gate electrode 39. Network 66 comprises a detector diode 68 and a video amplifier 70. A resistor 72 may be connected between network 66 and battery 46 to isolate the feedback signal from the dc voltage. In the operation of FETs in the saturated condition, in particular, feedback network 66 augments the biasing of FET 44, to reduce the power output variation 30 (FIG. 2). Such a feedback network may result in a lesser number of limiter stages required to achieve a desired power output variation 30 than in a cascaded amplifier without a feedback network.

In FIG. 4(*c*) there is shown a modified arrangement of the biasing configuration of 4(*b*). In this arrangement of FIG. 4(*c*), the feedback network 66 is connected between second gate electrode 39 and drain electrode 54 of successively cascaded FETs 44 and 50. The output power can be further limited as a function of RF input drive by using such a form of the feedback network 66 as shown in FIG. 4(*c*). Here the RF output power of the succeeding (or later) FET 50 is detected and amplified to provide inverse feedback to second gate 39 of the preceding FET 44. Thus, an increase in power with drive causes the gain of FET 44 to be reduced. This in turn reduces or nullifies the increase in RF power, enhancing the limiting function.

The use of dual-gate FETs provides desirable functional advantages over the known prior art devices, in particular, the single gate FET. The dual-gate structure, which, in addition to increased gain and stability, has enhanced functions due to the presence of two independent control gates. A device having the second gate with a deeper pinch-off voltage has been found to exhibit noise, stability, and gain control characteristics at microwave frequencies. (For a further explanation of dual gate FETs see "Single-and Dual-Gate GaAs Schottky-Barrier FET's for Microwave Frequencies," by S. Asai, H. Kurono, S. Takahaski, M. Hirao and H. Kodera, Proc of the 5th Conf., (1973 International) on Solid State Devices, Tokyo, 1973, Supplement to the Journal of the Japan Society of Applied Physics, Vol. 43, 1974 and "Performance of Dual-Gate GaAs MESFETs as Gain-Controlled Low-Noise Amplifiers and High Speed Modulators," by G. A. Liechti, ISSCC 75, WPM 7.2, Feb. 12, 1975.) In the dual gate FET, gate 39 is biased to achieve a desirable gain level and saturation operation while the input RF signal is applied to the other gate 38. The dual gate device significantly reduces the capacitance between the signal input gate 38 and drain electrode 40 over an equivalent single-gate device. This provides for an increased small-signal gain per stage compared to a single-gate device having an equivalent gate length. The reduction in the capacitance also decreases direct RF feedthrough from input to output which enhances the overdrive or saturation characteristics of the FET.

A dual gate GaAs FET power limiter has been tested, the limiter comprising a small signal amplifier 12 of three stages and a saturated amplifier 16 of four stages. The limiter was arranged to operate in C-band, and more particularly, a 5 GHz. The limiter was driven over an input power range from 0 to +15 mW and the small signal amplifier was biased to have a small signal gain of approximately 7 db. Under these operating conditions, the limiter exhibited a gain of unity at point 29 as shown in FIG. 2 where the input drive level and thereby the power output was about 6 mW. At this drive level and beyond, the compressive slope of the limiter (given by $\Delta Pi/\Delta Po$) was 9 mW/0.3 mW or 14.8 db. Such a limiter can achieve a power output variation within 0.025% of the input power variation to obtain a frequency accuracy of 1 MHz in a 4 GHz bandwidth for use in frequency discriminator applications. This is equivalent to an incremental power output fluctuation of 1 part in 4000, i.e., 36 db down from saturation over the total variation in the input drive range. Assuming an input drive range of 31 db, the combined value of input power swing and output limiting is equivalent to an overall compression ratio of 67 db. Such an FET limiter requires no circulators or isolators since the amplifier stages use three-terminal devices as straight through amplifiers resulting in considerably improved fine grain structure and simplification of circuitry.

What is claimed is:

1. A power limiter for generating an output RF signal of substantially constant power level in response to an input RF signal of varying power level, comprising:

a field effect type transistor having first and second gate, drain and source electrodes, said first gate electrode being receptive of said input RF signal;

means for biasing said second gate electrode of said transistor such that said transistor operates in a gain region characterized by a power curve having a slope whose change in output power is substantially equal to or greater than the change in input power, and a saturation region characterized by a power curve having a compression slope whose change in output power is substantially less than the change in input power, such that the final output power variation is small compared to the input power variation,

said substantially constant output RF signal being generated over said saturation region.

2. A power limiter according to claim 1, further including a feedback circuit connected between said drain and said second gate electrodes to provide a predetermined voltage to said transistor to reduce said final output power variation.

3. A power limiter for generating an output RF signal of substantially constant power level in response to an input RF signal of varying power level, comprising:

a first multistage amplifier responsive to said input RF signal for generating a first output RF signal;

a second multistage amplifier responsive to said first output RF signal for generating a second output RF signal;

each of said frist and second amplifiers including field effect type transistors each having first and second gate, drain and source electrodes in each stage, said transistors of each amplifier being connected in cascaded arrangement such that the first gate electrode of a succeeding transistor is connected to the drain electrode of a preceding transistor;

means for biasing said second gate electrodes of said transistors of said first amplifier to produce a predetermined gain level of said first output RF signal; and

means for biasing said second gate electrodes of said transistors of said second amplifier such that said second amplifier is operated in a saturated condition at the gain level of said first output RF signal, such that said second output RF signal is substantially constant with said varying input RF power and the final output power variation is small compared to the input power variation.

4. A power limiter according to claim 3, further including a feedback circuit between the second gate and drain electrodes of each transistor of said second amplifier to provide a predetermined voltage of each transistor to reduce said final output power variation.

5. A power limiter according to claim 3, further including a feedback circuit between the second gate electrode of a preceding transistor and the drain electrode of a succeeding transistor of said second amplifier to provide a predetermined voltage to said preceding transistor to reduce said final output power variation.

* * * * *

APPENDIX D

United States Patent [19]

Mawhinney et al.

[11] **4,162,412**

[45] **Jul. 24, 1979**

[54] **MICROWAVE POWER LIMITER COMPRISING A SINGLE-GATE FET**

[75] Inventors: **Daniel D. Mawhinney; Herbert J. Wolkstein**, both of Livingston; **Arye Rosen**, Cherry Hill, all of N.J.; **Zygmond Turski**, Selden, N.Y.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **838,656**

[22] Filed: **Oct. 3, 1977**

[51] **Int. Cl.**[2] **H03G 11/04; H04B 3/04**

[52] **U.S. Cl.** ..... 307/237; 307/264; 328/171; 328/172; 333/17 L

[58] **Field of Search** ..... 307/264, 237; 333/17 L; 328/169-172

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,079,325 3/1978 Mawhinney et al. ..... 307/261 X

OTHER PUBLICATIONS

Fukuda et al., "A New Microwave Amplitude Limiter Using GaAs Field Effect Transistor"; IEEE Microwave Theory and Techniques Conf.; Jun. 1977.

Int'l Microwave Symposium; 6/1977, in *Microwaves* (pub.), pp. 9-10.

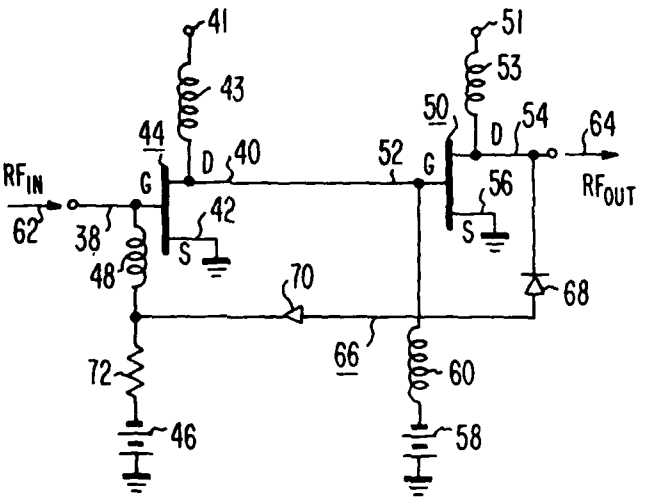
Primary Examiner—Larry N. Anagnos

Attorney, Agent, or Firm—H. Christoffersen; Joseph D. Lazar; Robert M. Rodrick

[57] **ABSTRACT**

A microwave power limiter for generating an output RF signal of substantially constant power level in response to an input RF signal of varying power level comprises a single gate field effect transistor (FET). The FET is biased such that the RF power output variation is small compared to the input power variation in the saturation region. A number of FET cascaded stages may be utilized to reduce this power output variation. A small signal amplifier including a number of FET cascaded stages may be employed in the limiter to increase the power level to that gain or drive level compatible with the saturated FET stages.

3 Claims, 9 Drawing Figures



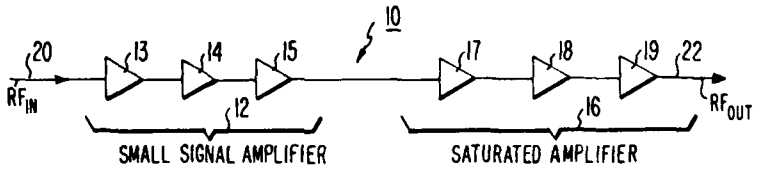


Fig. 1

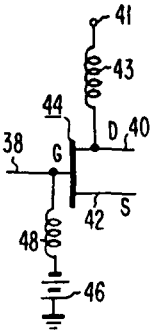


Fig. 4a

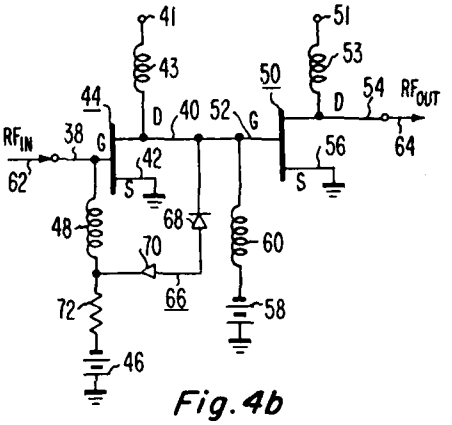


Fig. 4b

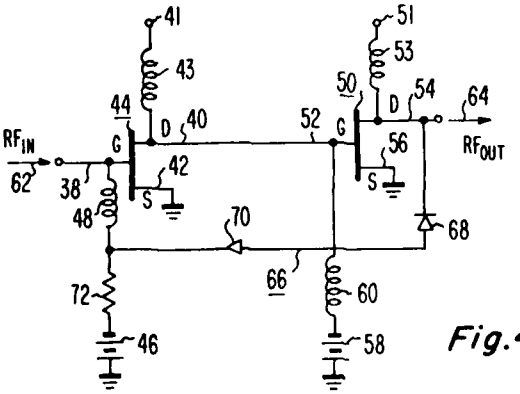


Fig. 4c

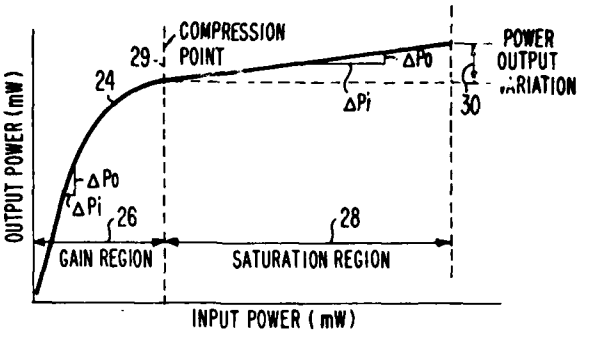


Fig. 2

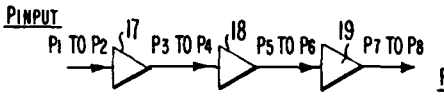
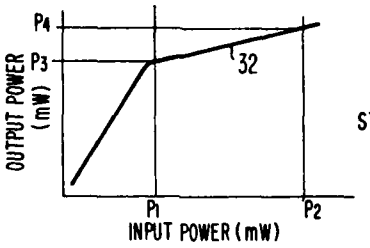
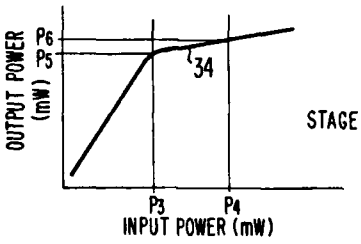


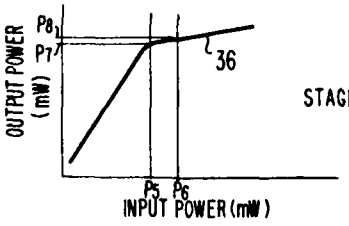
Fig. 3a



STAGE 17 Fig. 3b



STAGE 18 Fig. 3c



STAGE 19 Fig. 3d

MICROWAVE POWER LIMITER COMPRISING A SINGLE-GATE FET

The Government has rights in this invention pursuant to Contract No. N00039-74-C-0227 awarded by the Department of the Navy.

CROSS REFERENCE TO RELATED APPLICATIONS

Of interest is the following copending application Ser. No. 838,720, filed on Oct. 3, 1977, entitled "Microwave Power Limiter Comprising a Dual-Gate FET", based on the invention of Herbert J. Wolkstein, Arye Rosen and Jitendra Goel and assigned to the same assignee as is the present invention.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a microwave power limiter and, more particularly, to a power limiter including a single gate field effect transistor.

2. Description of the Prior Art

Many commercial and military systems require a source of constant RF power while simultaneously tolerating a wide variation of RF input power to the same system. It is often a system requirement that this fixed output power level be obtained over a wide frequency bandwidth. Such a power limiter having these desirable characteristics may be used as an RF amplifier, front end receiver where fixed output power is necessary for radar terrain mapping and associated video oscilloscope displays. Other limiter applications include receivers that are used for phase and frequency identification for electronic countermeasure (ECM) systems. In this application, fixed input power is generally applied to phase discriminators for accurate conversion of frequency (or phase) into an output dc voltage. A limiter having these properties may also be utilized for bi-phase and digital communications systems where coded binary signals are received and cannot be reconstructed to constant power output levels independent of the amplitude variations ... the receiving antenna.

One of the conventional approaches for achieving constant (or standardized) output power, independent of drive variation and frequency, is to utilize a multistage high gain amplifier chain. This amplifier chain is designed to constrain operation of several of the output stages to the overdriven or saturation region where the output power swing is greatly compressed in spite of large variations in the input power range to the chain. Both bipolar silicon transistors and tunnel diode amplifiers (TDA) are used in such multistage limiters. The bipolar transistor limiter is restricted, however, to low frequency applications and is not often selected for use. For other limiting amplifier circuits see U.S. Pat. No. 3,940,704 issued Feb. 24, 1976 and U.S. Pat. No. 3,999,084 issued Dec. 21, 1976 both of which use operational amplifiers and U.S. Pat. No. 3,932,768 issued Jan. 13, 1976 and U.S. Pat. No. 4,008,440 issued Feb. 15, 1977 both of which utilize differential amplifiers.

The TDA is in wide use and has heretofore provided desirable amplifier-limiter capabilities. The TDA limiter suffers, however, from diverse problems and disadvantages, limiting the applications and performance of the TDA limiter. For instance, the power output for a broadband TDA is limited to levels of about −6 dbm (0.25 mW) or less. This power output level produces an RMS output voltage of less than 0.1 volt, with a video detector circuit having an impedance of 100 ohms. Such an output is too low to drive a conventional phase interferometer-discriminator and detector without the use of video amplifiers. Another disadvantage of the TDA is that, since it is a two terminal device used as a reflection amplifier, circulators for each stage and isolators between every other stage are needed for stability of the limiter. Such a multiplicity of interconnected components typically utilizing ferrite materials produces many reflections which add in-and-out-of-phase resulting in considerable fine and coarse grain structure which directly reduces the accuracy when used with a discriminator. In such a discriminator system, for example, a variation of about 0.1 db will cause an attendant error of approximately 80 MHz in a 4 GHz band system. Furthermore, the use of necessary circulators and isolators in a multistage TDA configuration requires extensive circuitry and thereby, a relatively costly device.

SUMMARY OF THE INVENTION

According to the present invention, a power limiter generates an output RF signal of substantially constant power level in response to an input RF signal of varying power level. The limiter comprises a field effect type transistor having gate, drain and source electrodes. Included in the limiter is means for biasing the transistor such that the transistor operates in a gain region characterized by a power curve having a slope whose change in output power is substantially equal to or greater than the change in input power. The transistor also operates in a saturation region characterized by a power curve having a compression slope whose change in output power is substantially less than the change in input power such that the final output power variation is small compared to the input power variation. The substantially constant RF signal is generated over the saturation region.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a diagrammatic representation of one embodiment of the invention showing a number of amplifier stages in cascaded arrangement.

FIG. 2 is a graph showing the output power versus the input power of the power limiter of the present invention.

FIG. 3(*a*) is a block diagram illustrating the cascaded arrangement and the power distribution between the stages of the saturated amplifier of the preferred embodiment of the present invention.

FIGS. 3(*b*) to 3(*d*) are curves graphically showing the power variation of the cascaded stages of FIG. 3(*a*).

FIGS. 4(*a*) to 4(*c*) are schematic representations of biasing arrangements utilized to bias the FETs of the amplifier stages in the limiter of FIG. 1.

DETAILED DESCRIPTION OF THE *PREFERRED EMBODIMENT*

Referring to the drawing, there is shown in FIG. 1, a microwave power limiter 10, comprising a multistage small signal amplifier 12 and a multistage saturated amplifier 16. Amplifiers 12 and 16 each comprise three stages, viz., 13, 14 and 15 and 17, 18 and 19, respectively, for purposes of illustration although any number of stages depending upon the desired operational characteristics of limiter 10 may be utilized. Stages 13, 14 and 15 of amplifier 12 and stages 17, 18 and 19 of ampli-

fier 16 are connected in cascaded arrangement and each stage includes a single-gate, field effect transistor (FET) as will be explained in detail. An input RF signal 20 of varying power level is received by amplifier 12. An output RF signal 22 of constant power level is generated by limiter 10 in accordance with the invention as the output of amplifier 16. The stages of amplifiers 12 and 16 are biased by suitable bias arrangements (not shown in FIG. 1), the biasing of the stages to be described more fully with respect to FIGS. 4a–4c.

As shown in FIG. 2, the FETs of the stages of amplifiers 12 and 16 are biased to have their output power vary as a function of input power in accordance with curve 24. FET characteristic power curve 24 has a gain region 26 and a saturation region 28. In gain region 26 the slope of curve 24 is such that the change in output power (ΔPo) is equal to or greater than the change in input power (ΔPi). In the saturation region 28 the slope of curve 24 is such that the change in output power (ΔPo) is substantially less than the change in input power (ΔPi). Over the saturation range 28, the output power of the FET is constant within a power output variation 30. As with conventional amplifiers operating in the saturated condition for limiter applications, the slope of curve 24 in the saturated region 28 is commonly referred to as the "compressive slope" or the power compression ratio of the limiter. As known in the limiter art, the compressive slope is expressed as the input power drive variation versus the output power change, or ΔPi/ΔPo.

For power limiter applications, it is desirable to reduce the power output variation 30 to a minimum. The change in output power for an ideal power limiter is zero for changes in input power. Practical factors, such as bias voltages, FET configuration, FET circuitry and the FET material properties, typically limit the achievement of an ideal limiter, generally resulting in a certain amount of power output variation (30) in an individual limiter stage. Cascading of a number of FET stages and operating the FET stages in a saturated or overdriven condition will reduce the final output variation 30 to a level less than that variation for a single stage. By referring to FIG. 3, such a cascaded arrangement may be more fully understood.

In the cascaded arrangement of FIG. 3(*a*), stages 17, 18 and 19 of saturated amplifier 16 are connected such that output power range (P_3 to P_4) of stage 17 is the input power range to stage 18, and the output power range (P_5 to P_6) of stage 18 is the input power range to stage 19. Power range P_3 to P_4 and range P_5 to P_6 are the output power variations of stages 17 and 18, respectively. P_1 to P_2 is the input power range to stage 17 as received from the output of small signal amplifier 12. P_7 to P_8 is the final power output variation as the output signal of stage 19. Curves 32, 34 and 36 represent the characteristic curves of the FETs of stages 17, 18 and 19 respectively as shown in FIGS. 3(*b*), 3(*c*) and 3(*d*). By applying the output of a preceding stage as the input of a succeeding stage as the FETs are operated in a saturated condition in which the change in output power is less than the change in input power, the final power output variation, e.g., P_7 to P_8, can be reduced, as shown graphically in FIGS. 3(*b*) through 3(*d*). In such a cascaded arrangement the final power output variation can be reduced even further by adding more stages. It should be appreciated, however, that depending upon the power output variation tolerable in a particular limiter operation, cascaded FET stages may not be needed, the output of a single stage being satisfactory.

In the preferred embodiment shown in FIG. 1, small signal amplifier 12 is utilized to produce a power level which is compatible with the desired power level of saturated amplifier 16. The FETs of each of the stages 13, 14 and 15 are biased to operate in the gain region 26 as shown in FIG. 2 such that the change in output power is equal to or greater than the change in input power. By cascading stages operating in the gain region such that the output of a preceding stage provides the input of a succeeding stage the gain level of the final output stage 15 can be increased over the gain level to the input stage 13. It should be understood that the gain level provided by small signal amplifier 12 to saturated amplifier 16 can be changed by increasing or decreasing the number of stages. It should also be appreciated that small signal amplifier 12 may be eliminated in a system where the gain level of the RF input signal 20 is compatible with the gain level of the saturated amplifier 16.

Each of the FETs in the stages of amplifiers 12 and 16 have gate 38, drain 40 and source 42 electrodes as shown schematically on FET 44 in FIG. 4(*a*). In the preferred embodiment, FET 44 is a Gallium Arsenide (GaAs) metal semiconductor field effect transistor (MESFET), although other field effect type transistors such as, for example, junction field effect transistors (JFET), wherein the current is controlled by an electric field, may also be used. FET 44 may be biased by applying a dc voltage to gate electrode 38 as by battery 46 through an inductor 48. The other terminal of battery 46 may be grounded. Biasing of FET 44 may also be achieved by pulsed voltages as well as by dc voltages. Drain electrode 40 is biased by applying a suitable voltage to terminal 41 through an inductor 43, for example.

A biasing arrangement for cascaded FETs is shown in FIG. 4(*b*). For example, FET 44 with the biasing circuit as shown in FIG. 4(*a*), may be cascaded with an FET 50 of a succeeding stage. FET 50 has gate 52, drain 54 and source 56 electrodes. Drain electrode 40 of FET 44 is connected to gate electrode 52 of FET 50 and the source electrodes 42 and 56 respectively of each FET 44 and 50 are grounded. A battery 58 provides a predetermined dc voltage to gate electrode 52 through an inductor 60, the other terminal of battery 58 being grounded. The drain electrode 54 is biased by applying a suitable voltage to terminal 51 through inductor 53, for example. An input RF signal 62 may be applied at gate electrode 38 and an output RF signal 64 generated at drain electrode 54. In the preferred embodiment of the invention, a feedback network 66 is connected between the drain electrode 40 and gate electrode 38 of each of the FETs utilized. Feedback circuit 66 feeds a portion of the output signal from drain electrode 40 back as an input signal to gate electrode 38. Network 66 comprises a detector diode 68 and a video amplifier 70. A resistor 72 is connected between network 66 and battery 46 to isolate the feedback signal from the dc voltage. In the operation of FETs in the saturated condition, in particular, feedback network 66 augments the biasing of FET 44, to reduce the power output variation 30 (FIG. 2). Such a feedback network may result in a lesser number of limiter stages required to achieve a desired power output variation 30 than in a cascaded amplifier without a feedback network.

In FIG. 4(*c*) there is shown a modified arrangement of the biasing configuration of 4(*b*). In this arrangement of FIG. 4(*c*), the feedback network 66 is connected

between gate electrode 38 and drain electrode 54 of successively cascaded FETs 44 and 50. The output power can be further limited as a function of RF input drive by using such a form of the feedback network 66 as shown in FIG. 4(c). Here the RF output power of the succeeding (or later) FET 50 is detected and amplified to provide inverse feedback to gate 38 of the preceding FET 44. Thus, an increase in power with drive causes the gain of FET 44 to be reduced. This in turn reduces or nullifies the increase in RF power, enhancing the limiting function.

The single-gate FET power limiter has been tested, the limiter comprising a small signal amplifier 12 of 5 stages and a saturation amplifier of 7 stages. The limiter was arranged to operate in X-band, and more particularly, at 10 GHz. The limiter was driven over an input power varying from 0 to +80 mw and the small signal amplifier was biased at a drain voltage of 8 V and a zero gate voltage to have a small signal gain of approximately 3.68 db. Under these operating conditions, the limiter exhibited a gain of unity at point 29, as shown in FIG. 2, where the input drive level and thereby the output power was about 60 mw. At this drive level and beyond, the compressive slope of the limiter (given by ΔPi/ΔPo) was 5.7 db. Such a limiter can achieve a power output variation within 0.025% of the input power variation to obtain frequency accuracy of 1 MHz in a 4 GHz bandwidth for use in frequency discriminator applications. This is equivalent to an incremental power output fluctuation of 1 part in 4000, i.e., 36 db down from saturation over the total variation in the input drive range. Assuming an input drive range of 31 db, the combined value of input power swing and output limiting is equivalent to an overall compression ratio of 67 db. Such an FET limiter requires no circulators or isolators since the amplifier stages use three-terminal devices as straight through amplifiers resulting in considerably improved fine grain structure and simplification of circuitry.

What is claimed is:

1. A power limiter for generating an output RF signal of substantially constant power level in response to an input RF signal of varying power level, comprising:

a field effect type transistor having gate, drain and source electrodes;

means for biasing said transistor such that said transistor operates in a gain region characterized by a power curve having a slope whose change in output power is substantially equal to or greater than the change in input power, and a saturation region characterized by a power curve having a compression slope whose change in output power is substantially less than the change in input power, such that the final output power variation is small compared to the input power variations; and

feedback circuit means connected between said drain and gate electrodes to provide a predetermined voltage to said gate electrode to reduce said final output variation;

said substantially constant output RF signal being generated over said saturation region.

2. A power limiter for generating an output RF signal of substantially constant power level in response to an input RF signal of varying power level, comprising:

a first multistage amplifier responsive to said input RF signal for generating a first output RF signal;

a second multistage amplifier responsive to said first output RF signal for generating a second output RF signal;

each of said first and second amplifiers including one or more field effect type transistors each having gate, drain and source electrodes, said transistors of each amplifier being connected in cascaded arrangement;

means for biasing said transistors of said first amplifier to produce a predetermined gain level of said first output RF signal;

means for biasing said transistors of said second amplifier such that said second amplifier is operated in a saturated condition at the gain level of said first output RF signal, such that said second output RF signal is substantially constant with said varying input RF power and the final output power variation is small compared to the input power variation; and

feedback circuit means between the gate and drain electrodes of each transistor of said second amplifier to provide a predetermined voltage to each transistor to reduce said final output power variation.

3. A power limiter for generating an output RF signal of substantially constant power level in response to an input RF signal of varying power level, comprising:

a first multistage amplifier responsive to said input RF signal for generating a first output RF signal;

a second multistage amplifier responsive to said first output RF signal for generating a second output RF signal;

each of said first and second amplifiers including one or more field effect type transistors each having gate, drain and source electrodes, said transistors of each amplifier being connected in cascaded arrangement;

means for biasing said transistors of said first amplifier to produce a predetermined gain level of said first output RF signal;

means for biasing said transistors of said second amplifier such that said second amplifier is operated in a saturated condition at the gain level of said first output RF signal, such that said second output RF signal is substantially constant with said varying input RF power and the final output power variation is small compared to the input power variation; and

feedback circuit means between the gate electrode of a preceeding transistor and the drain electrode of a succeeding transistor of said second amplifier to provide a predetermined voltage to said preceeding transistor to reduce said final output power variation.

* * * * *

APPENDIX E

A Novel FET Frequency Discriminator*

A. Rosen, D. Mawhinney, and L. S. Napoli

RCA Laboratories, Princeton, N. J. 08540

Abstract–We have developed wideband GaAs FET microwave frequency discriminators that are smaller and perform better than the conventional interferometer type. The new discriminators consist of a 1.0 × 1.3-cm thin-film ceramic circuit on which are mounted a GaAs FET chip and an Si beam-lead Schottky diode. A typical discriminator instantaneously covers the frequency range from 7 to 11 GHz, producing a dc output voltage ranging from approximately −200 MV at 7 GHz to +300 MV at 11 GHz for an input of 0.2 mV. Compared to the interferometer-type discriminators, the FET discriminators provide approximately 10 times larger output voltages for the same rf input.

Introduction

One important application for wideband microwave discriminators is in frequency memory systems, where the device is used to provide an accurate analog voltage related to frequency for open-loop VCO set-on or closed-loop VCO frequency control. For either function, a linear relation between input frequency and output voltage is desirable but not essential. The use of post-detection voltage processing or linearization can compensate for overall nonlinearity to a considerable degree. In this paper we describe a novel FET discriminator consisting of an integrated microwave GaAs FET chip and an Si beam-lead Schottky diode. The high frequency gain roll-off of the FET augmented by an

* The research reported in this paper was sponsored in part by the Naval Electronic System Command, Washington, D C., under Contract No. N00039-76-C-0280 and RCA Laboratories, Princeton, N.J.

input shaping network and biasing networks, provided the desired wideband discriminator characteristic.

Techniques for the rapid and accurate determination of unknown signal frequencies are of considerable interest in modern military electronic systems. A microwave interferometer employing 3-dB hybrid couplers to split and later recombine the incoming signal after transmission through unequal path lengths is frequently used for this application.

The FET discriminator discussed in this paper provides a greater output voltage swing for a given limiter output power, less fine-grain structure, smaller volume, and potentially lower cost. The new discriminator consists of a 1.0 × 1.3 cm thin-film ceramic circuit on which are mounted a GaAs FET chip and an Si beam-lead Schottky diode. The Schottky diode detector is dc isolated from the FET drain circuit by a ceramic chip blocking capacitor, and is forward biased to a current of between 0.1 and 1.0 mA through a dropping resistor and an rf choke.

Basic Considerations

The discriminator circuit most widely used today is the passive interferometer type, shown schematically in Fig. 1. A preleveled rf signal is divided into two channels of unequal electrical length. The resulting

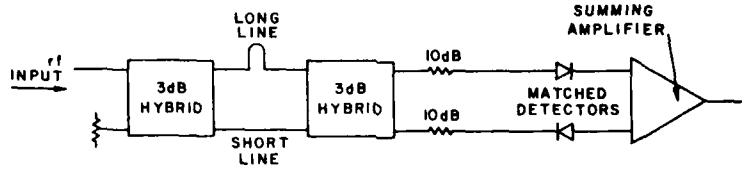


Fig. 1—Long-line/short-line pulse interferometer used for frequency discriminator.

signals, displaced in phase, are recombined and detected, resulting in a voltage output that is a function of the frequency of the input signal.[1-3] Problems with this type of device have been related to the need to very accurately match the various elements of the two paths–the hybrid couplers crystal detectors, diodes, connectors, etc. To ensure a frequency resolution of ±1 MHz in a 4-GHz band, mismatches of less than 1.05:1 in VSWR would be required, a figure that is not achievable in practice. In addition, input rf power variations across the band of interest must be restricted to a fraction of a dB, which places major constraints on the design of the limiter at the input of the discriminator circuit.

Even when the discriminator circuits are fabricated in MIC (micro-

wave integrated circuit) form, thereby greatly reducing the line length and eliminating many interconnection problems, a phase interferometer of this general design still produces a nonlinear frequency error equivalent to ±50 MHz in the 7 to 11-GHz band.[4] A different concept of a discriminator circuit is clearly required.

FET Discriminator Design Approach

A completely different approach to the problem of converting a pulsed microwave signal to a voltage that is an accurate measure of the microwave frequency is based on the utilization of the transfer function of a broadband microwave amplifier using GaAs Schottky-barrier field-effect devices.

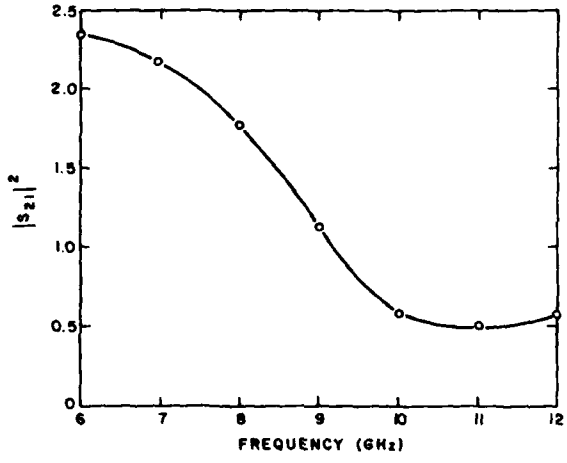


Fig. 2—Typical transfer function of untuned FET amplifier.

Fig. 2 shows a typical transfer function of an untuned GaAs FET amplifier. As can be seen, the output is a monotonic, although not linear, function of frequency. It is this intrinsic property of the FET amplifier that is utilized in the frequency-discrimination embodiment. Input and output shaping networks are designed (using computer optimization routines) to provide maximum linearity over the band of interest.

A discriminator based on this approach was designed and described by Z. Turski, D. Mawhinney, and I. Drukier.[5-8] Its performance is compared to that of an interferometer-type unit driven from the same limiter in Fig. 3. The figure also shows the output when the FET dis-

criminator is removed. The output curves of Fig. 3 depict some of the following basic characteristics of an FET discriminator:

(1) For a given frequency band and a given power input, the FET discriminator provides a greater voltage swing than does the interferometer type;
(2) Linearity of output can be achieved with proper matching networks at the input and output of the FET;
(3) The output of the discriminator reflects the irregularities of the limiter driving it.

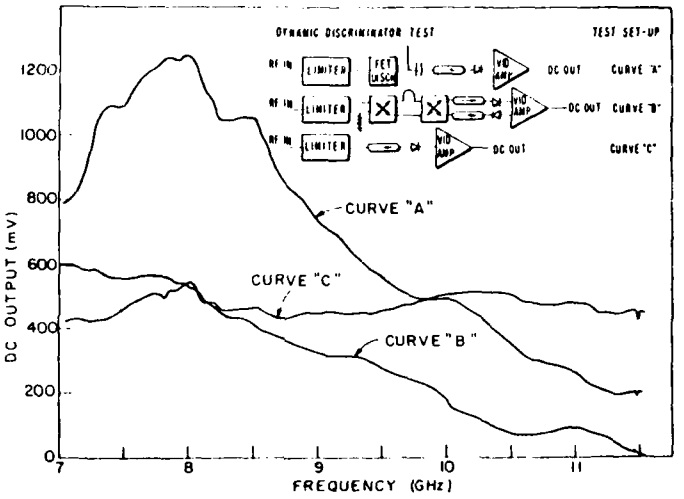


Fig. 3—Dynamic performance curves of early 8- to 11-GHz FET discriminator. Curve A is for active FET discriminator, B is for passive interferometer type discriminator, and C is the power feed through reference.

FET Discriminator Design Considerations

The basic discriminator circuit consists of a GaAs FET chip and an Si beam-lead Schottky detector diode mounted on a thin-film circuit on a ceramic substrate. The detector diode is dc-isolated from the FET drain circuit by a ceramic-chip blocking capacitor, and is forward biased to a current between 0.1 to 1.0 mA. Input and output response shaping for optimization of linearity and slope are utilized, but dissimilar approaches are employed in the FET input and output circuits, as explained below. A functional block diagram of the FET discriminator is shown in Fig. 4.

Table 1—Input and output scattering parameters of a typical FET chip for two values of drain voltage.

Frequency	S_{11}		S_{22}	
V_G = 0, V_D = 3V, I_D = 50 MA				
7000.0	.785	−148	.684	−87
7200.0	.760	−153	.671	−89
7400.0	.748	−161	.648	−91
7600.0	.751	−166	.642	−93
7800.0	.739	−170	.625	−96
8000.0	.736	−178	.604	−100
8200.0	.750	174	.583	−105
8400.0	.776	170	.564	−110
8600.0	.777	166	.550	−116
8800.0	.787	161	.549	−122
9000.0	.822	157	.556	−128
9200.0	.845	152	.562	−136
9400.0	.845	150	.568	−143
9600.0	.856	146	.585	−149
9800.0	.855	142	.602	−154
10000.0	.858	140	.620	−160
10200.0	.869	138	.642	−163
10400.0	.849	135	.664	−167
10600.0	.835	133	.685	−171
10800.0	.835	131	.703	−174
11000.0	.816	129	.719	−177
V_G = 0, V_D = 8V, I_D = 50 MA				
7000.0	.770	−152	.839	−82
7200.0	.743	−157	.831	−84
7400.0	.734	−165	.813	−86
7600.0	.740	−170	.813	−88
7800.0	.735	−174	.798	−91
8000.0	.731	177	.784	−95
8200.0	.744	170	.768	−99
8400.0	.771	166	.756	−104
8600.0	.775	162	.745	−109
8800.0	.786	157	.742	−115
9000.0	.812	153	.745	−121
9200.0	.837	149	.747	−128
9400.0	.839	147	.752	−134
9600.0	.851	143	.766	−140
9800.0	.850	139	.777	−145
10000.0	.856	137	.795	−151
10200.0	.865	135	.809	−156
10400.0	.843	132	.829	−160
10600.0	.829	130	.846	−165
10800.0	.827	128	.855	−167
11000.0	.807	126	.867	−171

FET Chip Characteristics

The basic concept of the FET discriminator requires the maximum gain of the active device only at the lowest frequency, while frequency roll-off characteristics are optimized to provide the desired output versus frequency performance. It was noted that varying the drain voltage of the FET results in considerable variations in the device output impedance, while maintaining a constant FET input impedance. An example of this effect is shown in Table 1, where S_{11} and S_{22} scattering parameters of a typical FET chip are shown for two values of device drain voltage (V_D = 3 and 8 V) over the 7- to 11-GHz frequency range. This property can be used to optimize the discriminator output circuit.

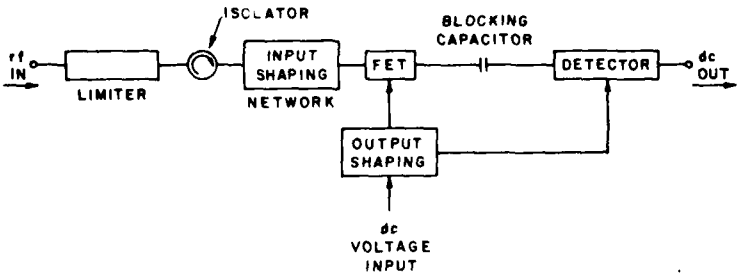


Fig. 4—Functional block diagram of FET discriminator.

Linearization And Slope Optimization

While a true linear relationship between input frequency and output voltage is usually not essential in most receiver subsystems (since post-detection voltage processing and linearization can be used), linear transfer characteristics are nevertheless highly desirable and frequently simplify circuit design.

Linearization of the discriminator characteristic is accomplished by shaping arrangements at the input and output of the FET chip. The input network uses the conventional approach of selecting a microwave matching circuit geometry and adjusting it for linear output with the aid of computer-aided optimization routines. For the output circuit, however, it was thought prudent to adjust the output of the FET by purely electronic means, as opposed to circuit-geometry approaches. The large FET output impedance variability as a function of drain voltage changes, discussed in the preceding section, provides such an adjustment

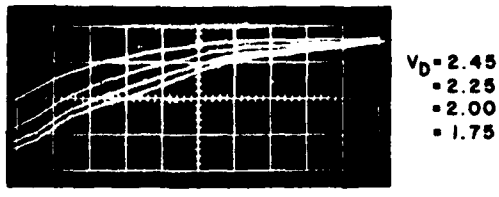


Fig. 5—Effect of drain voltage variation on FET discriminator output characteristics.

Fig. 6—Effect of detector bias on FET discriminator output characteristic.

mechanism. The elimination of an output-matching microwave transmission line helps to eliminate a source of multiple reflections and discontinuities that tend to introduce irregularities in the discriminator output characteristic. An example of the effect of drain-voltage variations on the discriminator output response is shown in Fig. 5. As can be seen, the most pronounced effect on the shape of the output curve is at the

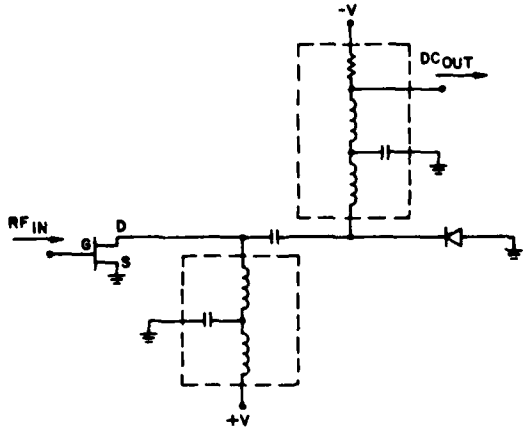


Fig. 7—Output shaping arrangements for FET discriminator.

low-frequency end of the band. In addition to changes in the linearity of the output curve, the slope can also be varied, so that the output voltage swing can be changed as a function of drain voltage.

Another means of affecting the shape of the discriminator output (as a function of input frequency) is afforded by adjustments in the forward-bias current of the detector diode, as shown in Fig. 6. Here, the greatest effect appears to take place at the high-frequency end of the operating band. Again, the adjustment affects both the slope and the linearity of the video output.

The effectiveness of these electronic adjustments and the apparent complementary nature of the two approaches (drain voltage affecting the lower frequencies, detector bias affecting the high-frequency end) led us to adopt the electronic "shaping" approach at the discriminator output, while using the more conventional microwave matching network at the FET input. The basic scheme is shown in Fig. 7.

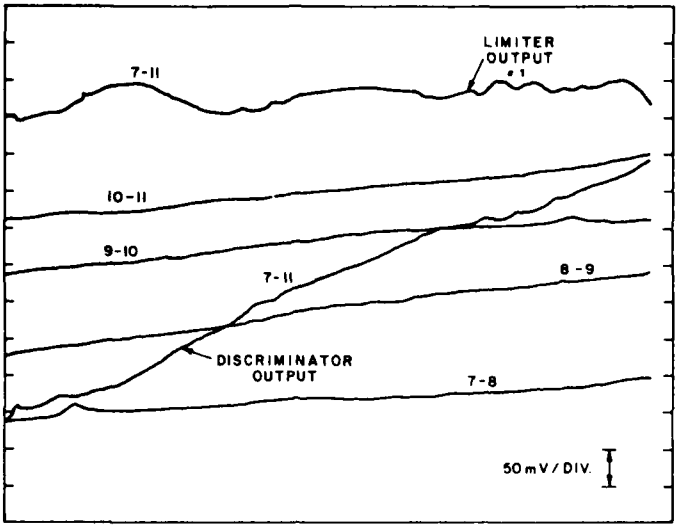
Effect Of Limiter Characteristics

The accuracy of power-leveling at the input to the discriminator can be expected to have a profound effect on the accuracy of frequency-to-voltage conversion, and the experimental data confirm the need for precise limiting of the input signal over the band of operation. The expanded x-y recorder plots of the limiter output and the discriminator response, shown in Figs. 8 (A) and 8 (B), clearly indicate the correspondence of the irregularities in the discriminator output to the imperfections in the limiting at its input. Indeed, it is the lack of smooth power leveling that actually limits the overall frequency band over which the FET discriminator can be used in a practical system. For instance, the final limiter–discriminator unit actually performs over the 7.5 to 11-GHz band (rather than the desired 7- to 11-GHz range) due to irregularities in the limiter performance in the 7- to 7.5-GHz region. While these considerations apply equally to interferometer- and FET-type discriminators, the crucial dependence of the broadband discriminator response on the excellence of limiting was less evident with the older designs, because it was masked by the multiple reflections in the short-line/long-line discriminator arrangements.

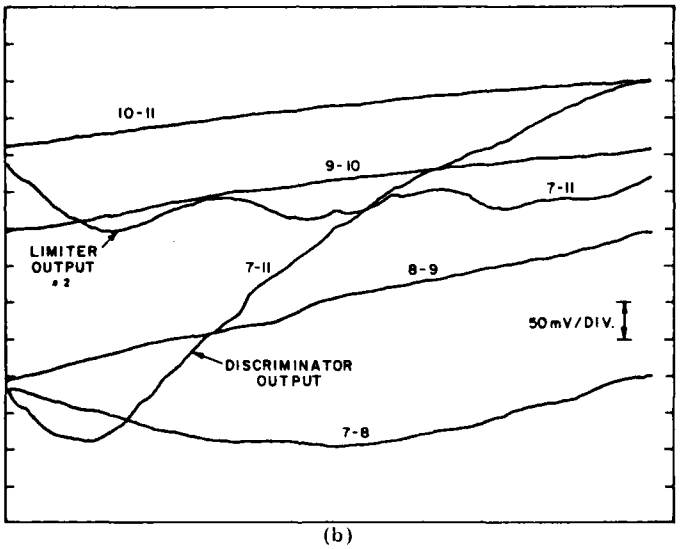
Experimental Results

A. Discriminator Circuit

A breadboard discriminator based on the approach outlined above has been tested. Fig. 9 is a photograph of the discriminator including integral



(a)



(b)

Fig. 8—Expanded x-y recorder plots showing effect on discriminator output of irregularities in limiter input: (a) for limiter #1 and (b) for limiter #2.

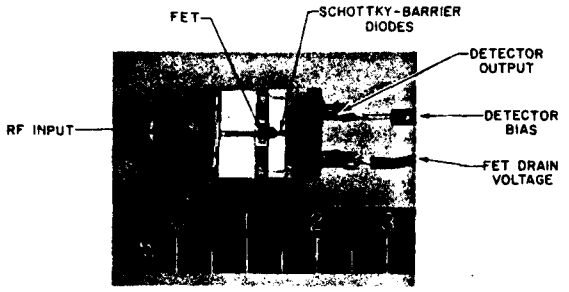
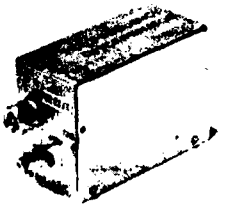
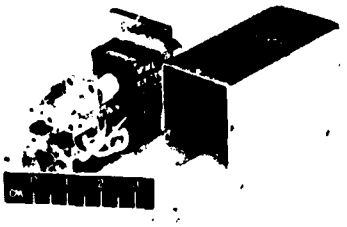


Fig. 9—FET descriminator.



(a)



(b)

Fig. 10—FET discriminator (a) packaged and (b) with cover removed showing circuit components.

detector; Fig. 10 shows both the packaged discriminator and a view of circuit contents with the cover removed. The overall assembly consists of an input isolator, the FET amplifier stage, detector, and MIC assembly, and a voltage regulator to stabilize the drain voltage.

The discriminator assembly unit, operating in conjunction with a TDA limiter,* operates over the frequency range 7.5 to 11 GHz (Fig. 11).

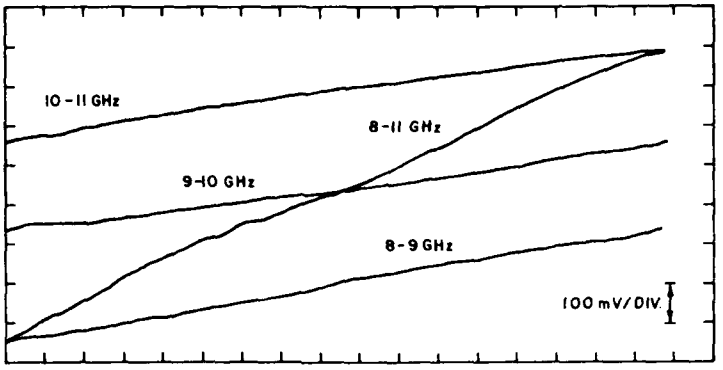


Fig. 11—FET discriminator operation (7.5 to 11 GHz).

B. Discriminator Noise Output

Measurements have been made to determine the video noise output of an FET discriminator. Fig. 12(a) shows the overall voltage output versus frequency. The intensified spot, expanded by a factor of 100 to 1 mV is shown in Fig. 12(b). The resulting noise level is measured by the width of the trace in Fig. 12(b), which is comparable to the width of the trace on the scope when the input is disconnected (Fig. 12(c)). The total frequency-noise equivalency of the measured noise voltage would therefore cause an estimated error of less than 1 MHz.

C. High-Frequency Unit

A unit designed around a GaAs FET device that has a maximum available gain in excess of 6 dB at 15 GHz was fabricated and tested over the 14.5- to 16.7-GHz frequency band. A special GaAs Schottky-barrier

* Aercom Model AL-78005 S/N 192.

detector developed by RCA[10] was employed in this discriminator. Performance is shown in Fig. 13 for three different matching adjustments. While these are preliminary results, they are very encouraging in terms of the monotonic output voltage versus input frequency at these short wavelengths.

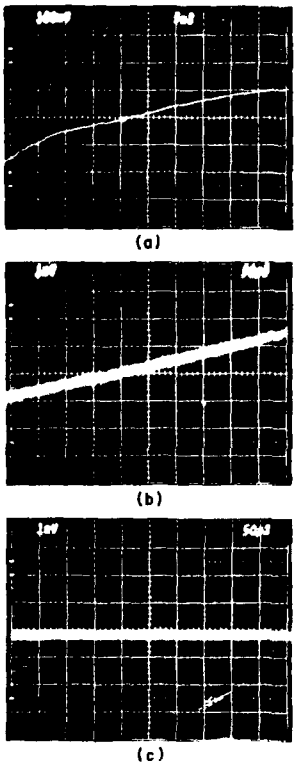


Fig. 12—FET discriminator output showing noise characteristics.

D. Discriminator Used in VCO Memory System

An early model of an FETdiscriminator was used in a locked-open-loop VCO frequency memory system. An interferometer-type discriminator which had been experimented with in that equipment, exhibited considerable fine-grain structure, which caused significant frequency error.

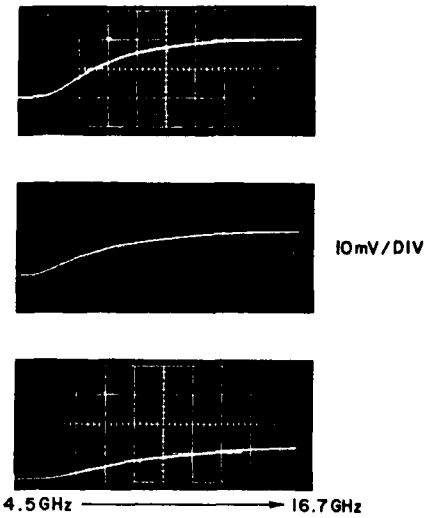


Fig. 13—Ku-band discriminator performance.

The FET discriminator that was used greatly reduced this error and provided, in addition, a larger output voltage swing.[9]

A comparison of the interferometer-type discriminator and an experimental version of an FET discriminator (without the integrated detector and isolator used in the final model of the system) is shown in Fig. 14. The dramatic reduction in size and weight is evident.

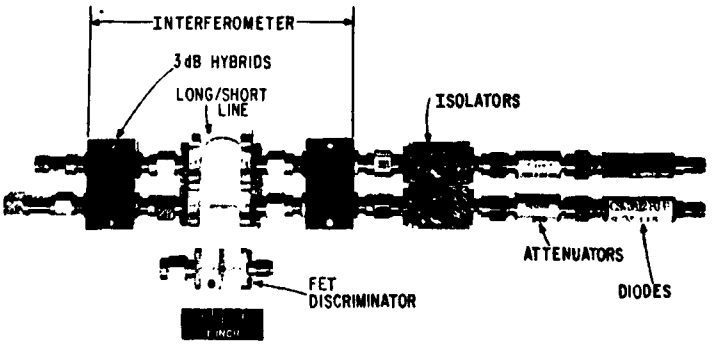


Fig. 14—Comparison of interferometer-type discriminator and FET discriminator circuit.

Although more recently fabricated FET discriminators have been improved in this respect, the output of the one installed in the frequency memory system departs considerably from a linear slope, but the change is smooth and gradual. Except for the bumps from the limiter in the region of 9.0 GHz, the FET discriminator is free from noticeable fine-grain structure, as shown by the oscilloscope photograph of Fig. 15(a). This shows the discriminator output for a swept frequency input from 8 to

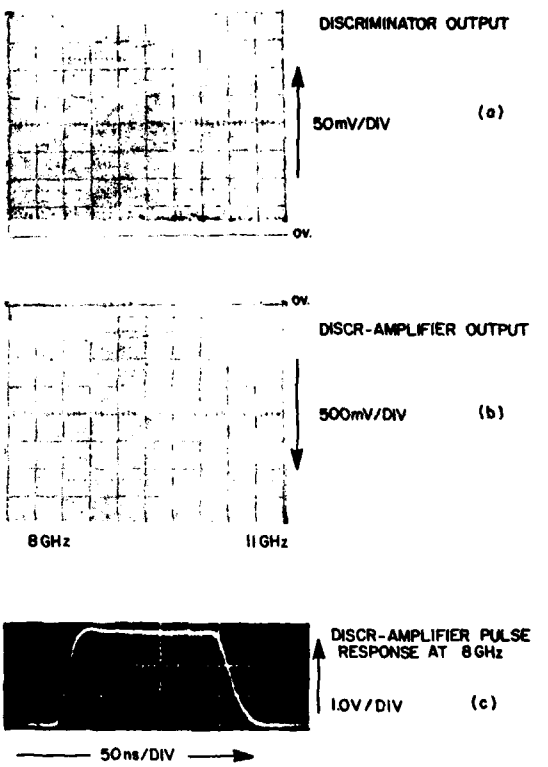


Fig. 15—*Discriminator performance* (VCO memory system unit).

11 GHz. The final adjustment of the drain voltage resulted in a voltage output swing of 160 mV for this same frequency range.

The FET discriminator is followed in the circuit by a video amplifier stage consisting of a high-speed hybrid operational amplifier set to a gain of approximately 17 to provide about a 2.5-V swing for driving the li-

nearizer through the follow-and-hold module. The swept output of the amplifier stage is shown in Fig. 15(b). and the pulse response is shown in Fig. 15(c) with the limiter/discriminator/amplifier combination driven by an 8-GHz, 250-ns input pulse. The extremely fast response capabilities of the FET discriminator are clearly demonstrated by these photographs.

Conclusions

A novel frequency discriminator suitable for use in EW receivers has been designed.

Compared to a dual-line MIC interferometer design, the FET discriminator provides higher output voltages, faster response time, better linearity, a smoother output response, and an inherently wider bandwidth. Moreover, its weight is less than one-third and its volume about one-quarter that of the interferometer-type unit.

A typical discriminator instantaneously covers the frequency range from 7 to 11 GHz producing a dc output-voltage swing of 500 mV.

Acknowledgments

The cooperation of the late J. Napoleon in providing the FET, and of E. Denlinger in providing the GaAs Schottky-barrier diodes is acknowledged with gratitude. In addition, the authors wish to express their appreciation to H. Wolkstein and W. W. Siekanowicz for critical review of this manuscript, and to E. Mykietyn for diligent circuit assembly and device testing.

References:

[1] R.J. Mohr, "Broadband Microwave Discriminator," IEEE Trans. Microwave Theory and Tech., 11, p. 263, July 1963.

[2] S.J. Robinson, "Comment on Broadband Microwave Discriminator," IEEE Trans. Microwave Theory and Tech., 12, p. 255, March 1964.

[3] L. I. Reber, "Improve Performance in Phase Discriminators," Microwaves, p. 48, May 1971.

[4] U.H. Gysel and J.P. Watjen, "MIC 7 to 11-GHz Frequency Discriminator," Final Report, Contract N00039-75-C-040 (Stanford Research Institute), Sept. 1976.

[5] Z. Turski, private communication.

[6] Patent pending No. 70,204, "Microwave Frequency Discriminator Comprising an FET Amplifier," Z. Turski and D. Mawhinney.

[7] Patent pending No. 70,221, "Microwave Frequency Discriminator Comprising a One Port Active Device," A. Rosen and Z. Turski.

[8] Patent pending No. 70,994, "Improved Microwave Frequency Discriminator Comprising an FET Amplifier," A. Rosen and L. Napoli.

[9] D.D. Mawhinney, "Locked-Open-Loop, VCO Frequency Memory System," Naval Electronic Systems Command, Final Report, Contract No. N00039-74-C-0227, Nov. 1976.

[10] E. Denlinger, S.G. Liu, H. Veloric, F. Duigon, and V. Lawson, "High Performance Mixer-Diode," Digest International Electron Devices Meeting, Washington, D.C., Dec. 1976.

APPENDIX F

DUAL-GATE MESFET VARIABLE-GAIN, CONSTANT-OUTPUT POWER AMPLIFIER

M. Kumar
RCA Laboratories
Princeton, New Jersey 08540

OCTOBER 1979
Bimonthly Report No. 6 for the period 18 July 1979
to 18 September 1979

Prepared for
Naval Research Laboratory
Washington, DC 20375

Contract No. N00173-78-C-0227

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) DUAL-GATE MESFET VARIABLE-GAIN, CONSTANT-OUTPUT POWER AMPLIFIER		5. TYPE OF REPORT & PERIOD COVERED Bimonthly Report No. 6 7-18-79 to 9-18-79
		6. PERFORMING ORG. REPORT NUMBER PRRL-79-CR-46
7. AUTHOR(s) Mahesh Kumar		8. CONTRACT OR GRANT NUMBER(s) N00173-78-C-0227
9. PERFORMING ORGANIZATION NAME AND ADDRESS RCA Laboratories Princeton, NJ 08540		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Research Laboratory Washington, DC 20375		12. REPORT DATE October 1979 13. NUMBER OF PAGES 19
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Variable-gain microwave amplifier
Dual-gate MESFET
Limiter
Microwave AGC amplifier

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes progress during Phase I of a two-phase effort to develop a constant-output broadband microwave amplifier based on a dual-gate MESFET stage. Three tasks described are (1) the development of a dual-gate MESFET stage using the second device gate for gain control; (2) the conceptual design of the overall amplifier; and (3) the development of an AGC loop involving the video amplifier.

DD FORM 1 JAN 73 1473

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20.

A breadboard amplifier was demonstrated operating over a 3-GHz band (4.5 to 7.5 GHz) and providing an output power of 0 dBm ±2.5 dB over its entire dynamic range of -40 dBm to 0 dBm of input power. For any fixed input power level within that range, the output power variation is within ±1.5 dB.

While the operation of the breadboard falls short of the ultimate program goal of a -50 dBm to 0 dBm dynamic range and output power of 0 dBm ±1 dB, the principle of a microwave AGC amplifier based on a dual-gate FET was nevertheless fully demonstrated. The final amplifier, to be built and delivered during Phase II of the program, is expected to meet the design specifications.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION I

INTRODUCTION

The objective of this program is the development of a linear variable gain constant output power amplifier with following specifications

Frequency :	4 to 8 GHz
Bandwidth :	3 GHz
Noise Figure :	7 dB (max)
Power Output :	0 dBm (min)
Output Power Variation :	$\pm$1 dB (max)
Dynamic Range :	-50 to 0 dBm, power input
Response Time :	<1 ns

The amplifier is required to have provisions for the following functions:

(a) The output rf power level of the amplifier settable as directed by the amplitude of an externally supplied dc input voltage.

(b) A separate port for direct amplifier cut-off and video gain control (pulsed control signal).

(c) A separate output port for supplying a video output signal derived from the amplifier's internal feedback leveling control.

The program was divided into two phases. Phase I is for demonstration of the feasibility of obtaining variable gain and constant output power on a breadboard model. Phase II requires the delivery of a final-packaged amplifier with provisions for processing input and output signals.

This report covers Phase I of this program, which comprises three major tasks. The first is to develop a dual-gate MESFET amplifier stage with second-gate control of amplifier gain. The second task is the conceptual design of the overall amplifier. The third task is to develop the AGC loop, which involves the video amplifier. This video amplifier is required to have high gain and large bandwidth to cover the dynamic range of the amplifier.

Considerable delay in delivery of the video amplifier from B & H Electronics* caused a delay in the program.

*B & H Electronics Co., Chester, NY.

SECTION II

DUAL-GATE FET AMPLIFIER STAGE

A single-stage amplifier was designed using an NEC 46300 dual-gate MESFET. We measured the S-parameters of the MESFET and then designed the input and output matching circuits. These matching circuits were designed for realizing maximum gain from gate 1 to drain for a given bias to the drain and the first gate, with the second gate grounded. The circuit design used the COSMIC program developed at RCA Laboratories for optimizing the network design.

A block diagram of the single-stage amplifier circuit is shown in Fig. 1. The amplifier was fabricated, and the rf performance was tested for gain as a function of the second-gate bias. Initially the amplifier design was made with the second gate terminated in 50 Ω. The gain performance of the amplifier is shown in Fig. 2 as a function of second-gate bias voltage. Figure 3 shows the variation of the gain as a function of frequency for different second-gate bias voltages. As seen from Fig. 3, a single-stage amplifier gain can be varied from -30 dB to 10 dB by changing the second gate bias from -3 V to 1 V.

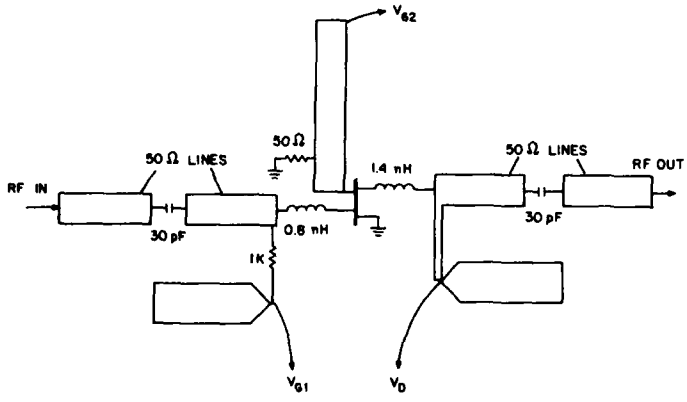


Figure 1. Matching networks for a dual-gate FET amplifier.

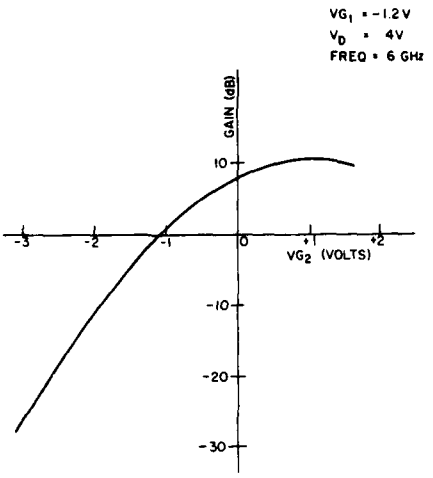


Figure 2. Variation of gain with second-gate bias (dual-gate amplifier).

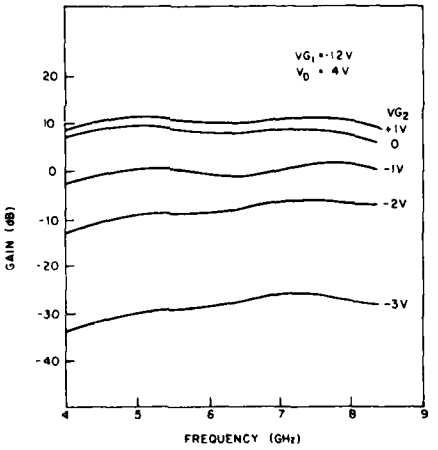


Figure 3. Variation of gain with frequency (dual-gate amplifier).

SECTION III

LINEAR AMPLIFIER AND AGC LOOP

The conceptual design of the amplifier is shown in Fig. 4. The first and last stages of the amplifier are fixed gain amplifiers, and the other three stages are advanced AGC control stages. The circuit configuration for one AGC control unit is depicted in Fig. 5. As shown in Fig. 5 the signal at the input of the amplifier is sampled through a coupler and is detected and processed at video frequencies to dynamically preadjust the gain of the amplifier. The detected signal is fed to the input of the video amplifier. The output of the video amplifier is fed to the second gate of the dual-gate FET amplifier.

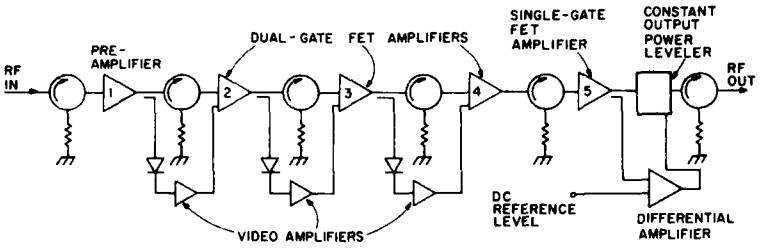


Figure 4. Conceptual design of the amplifier.

The distribution of power levels at different stages is shown in Table 1.

The next task was to look for a video amplifier having more than 50-dB gain and a response time of less than 1 ns. To meet these two requirements simultaneously is quite difficult. The best commercially available video amplifier has 25-dB gain and 300-ps rise time with a bandwidth of 2 kHz to 1.4 GHz. Three of these amplifiers were purchased from B & H Electronics, Inc. However, there was a considerable delay in the delivery of these amplifiers, resulting in a delay in testing. After performance testing of the amplifiers, our conceptual design of

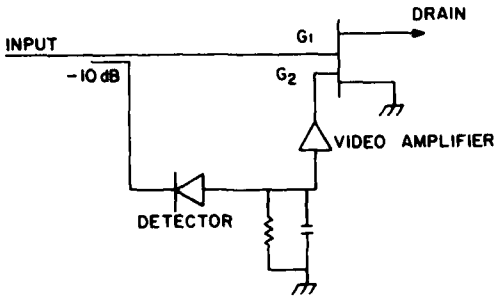


Figure 5. Advanced AGC control.

the amplifier was modified. The modified design is shown in Fig. 6. Since the gain of the video amplifier is less than that required to provide the voltage to the second gate of the dual-gate FET for controlling the gain, the input of the video amplifier was increased by using 3-dB couplers instead of 10-dB couplers and adding a single-gate FET amplifier (gain = 8 dB) to the AGC loop. This arrangement effectively provides the similar bias to the second gate of the dual-gate FET as was shown in Fig. 4. This arrangement (Fig. 6) uses three 3-dB couplers in the chain of 5 stages. This reduces the dynamic range of the linear amplifier from -50 dBm to 0 dBm to -40 dBm to 0 dBm. In order to provide sufficient drive for the AGC circuit, it was necessary to increase the output termination of the second gate (in the dual-gate FET stage) from 50 Ω to 1 kΩ, with the consequent reduction of the gain in that stage by 1 to 1.5 dB and of the overall amplifier gain by 3 to 4 dB.

TABLE 1. DISTRIBUTION OF POWER LEVELS AT DIFFERENT STAGES

Power input (dBm)	Preamplifier 1 Gain (dB)	Preamplifier 1 P_{out} (dBm)	Dual-Gate FET Amplifier 2 Gain (dB)	Dual-Gate FET Amplifier 2 P_{out} (dBm)	Dual-Gate FET Amplifier 3 Gain (dB)	Dual-Gate FET Amplifier 3 P_{out} (dBm)	Dual-Gate FET Amplifier 4 Gain (dB)	Dual-Gate FET Amplifier 4 P_{out} (dBm)	Single-Gate FET Amplifier 5 Gain (dB)	Single-Gate FET Amplifier 5 P_{out} (dBm)
-50	10	-40	10	-30	10	-20	10	-10	10	0
-40	10	-30	10	-20	10	-10	0	-10	10	0
-30	10	-20	10	-10	0	-10	0	-10	10	0
-20	10	-10	10	0	-10	-10	0	-10	10	0
-10	10	0	0	0	-10	-10	0	-10	10	0
0	10	10	-10	0	-10	-10	0	-10	10	0

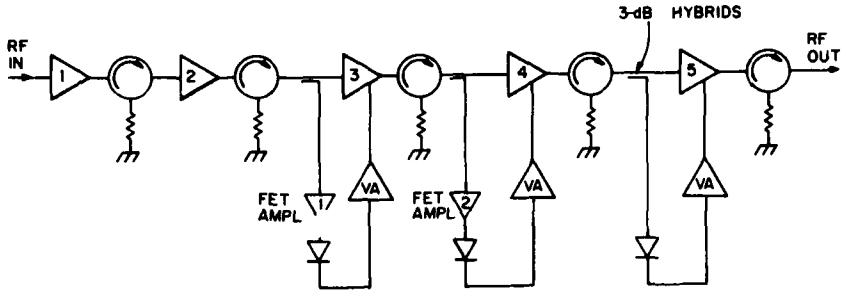


Figure 6. Block diagram showing the modified design.

SECTION IV

PERFORMANCE AND TEST RESULTS

A single-stage dual-gate FET amplifier with AGC is shown in Fig. 7. The rf performance of the amplifier was tested over the 4- to 8-GHz band with input power levels varying from -40 dBm to 0 dBm. Because of the lack of an rf pulse source having a pulse rise time of 1 ns, the testing was restricted to a rise time of 15 ns, using a HP-PIN diode modulator.

Figure 8 shows the rf input and output pulses of the amplifier on a sampling oscilloscope. As seen in Fig. 8, there is no degradation in the rise time of the pulse. Since the response time of the video amplifier is about 300 ps and that of dual gate FET is better than 200 ps, it is expected that the response time of the amplifier is less than 2 ns. Figure 9 shows the pulse response of the amplifier. The input pulse is shown in Fig. 9(a) and the output pulses at two different levels of input power, are shown in Figs. 9(b) and (c).

Figure 10 shows the variation of output power as a function of frequency for different input power levels of a single advanced AGC control unit (Fig. 6).

The variation of output power of the complete AGC amplifier as a function of frequency for different input power levels (-40 dBm to 0 dBm) is shown in Fig. 11. The variation of output power is within $\pm$2.5 dB in the frequency range of 4.5 to 7.5 GHz (3 GHz band) for variation in input power levels of -40 dBm to 0 dBm. It was discussed in Section III that the gain of amplifier at low input power levels is reduced by 3 to 4 dB because of problems in the second gate impedance. However, the variation of output power with frequency is within $\pm$1.5 dB for constant input power.

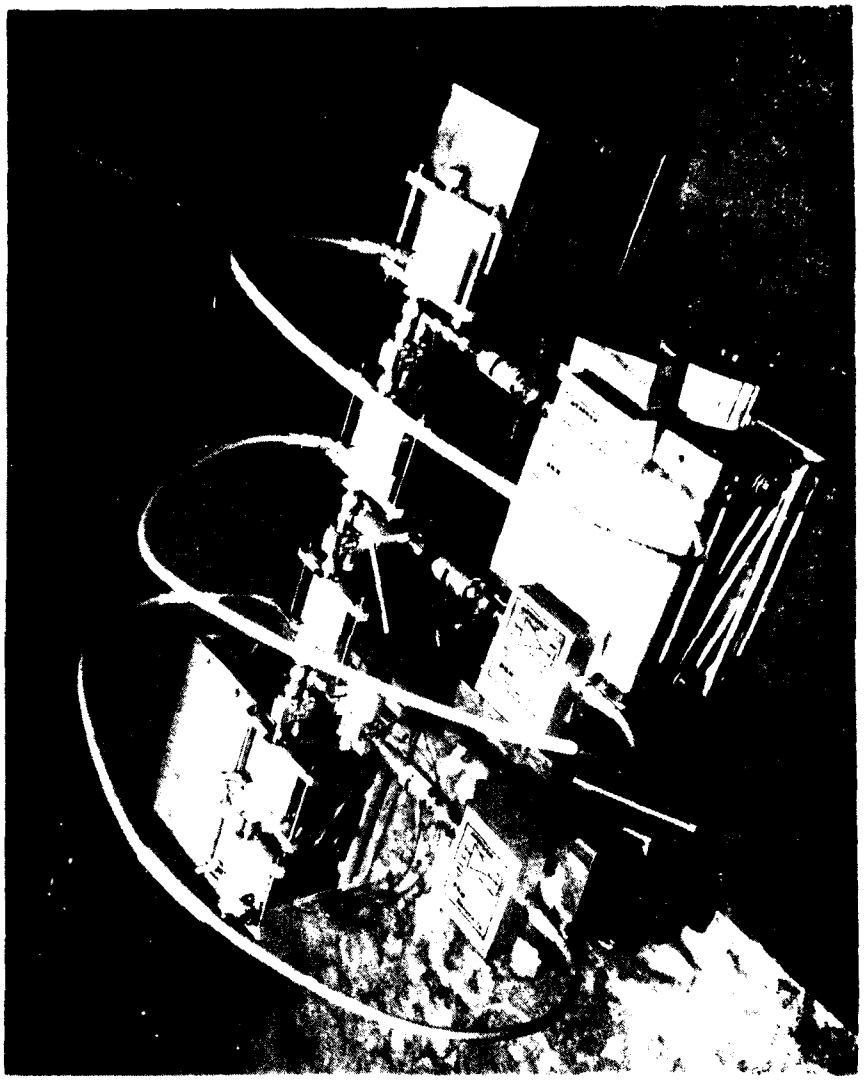
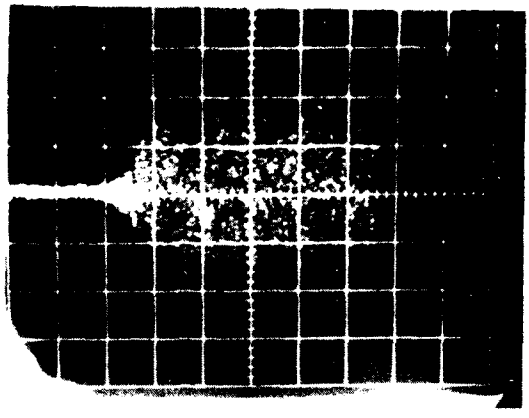
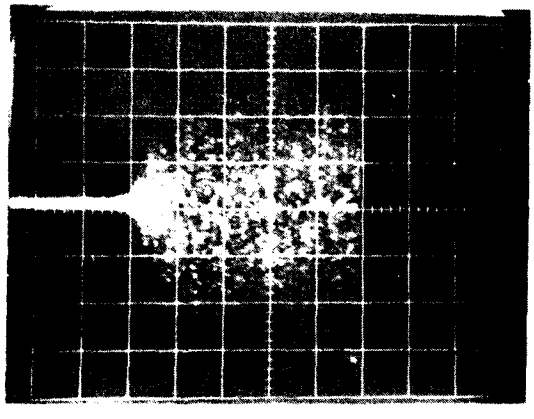


Figure 7. Photograph of the dual-gate FET amplifier with AGC.



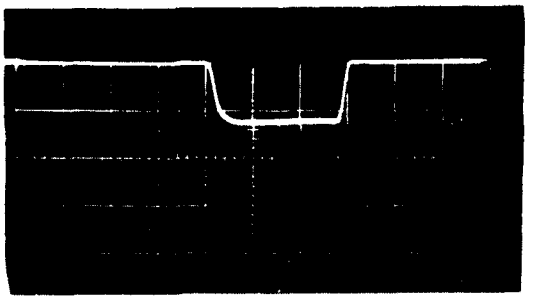
(a)



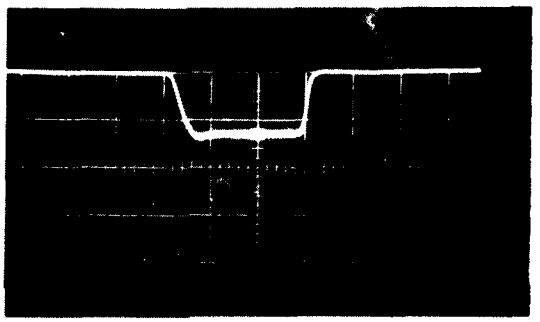
(b)

Figure 8. Amplifier rf input and output pulses.

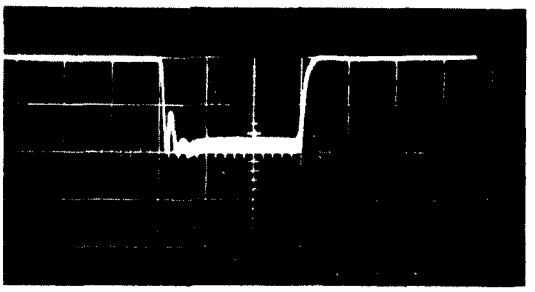
11



(a)



(b)



(c)

Figure 9. Pulse response of the dual-gate FET amplifier.

12

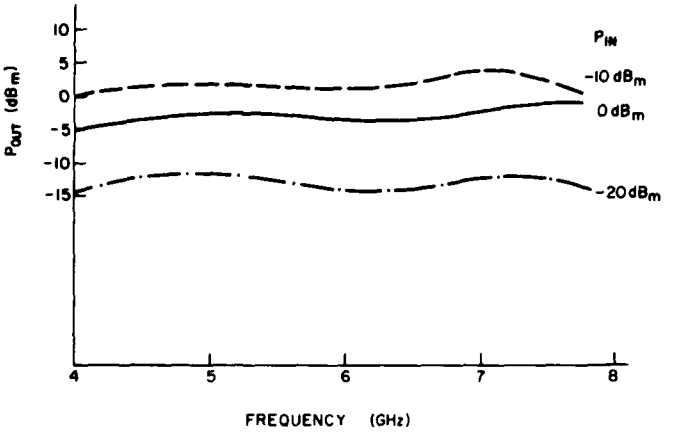


Figure 10. Variation of output power as a function of frequency and input power.

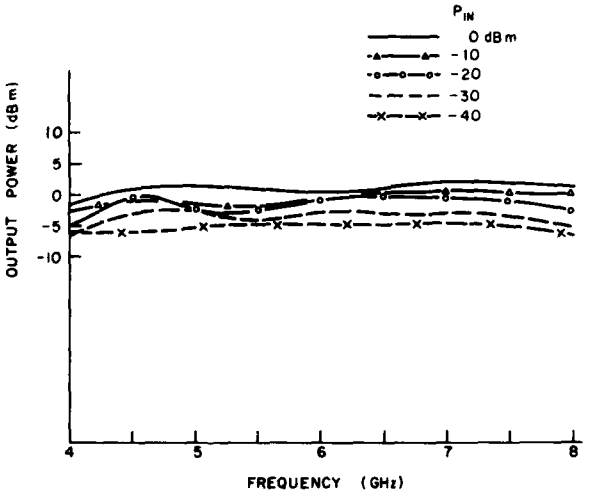


Figure 11. Output power of the complete AGC amplifier as a function of frequency and input power.

SECTION V

PLANNED IMPROVEMENTS

As seen from the results presented in Section IV, the performance of the amplifier needs to be improved to meet the specifications. The following improvements will be made before the final amplifier is delivered.

(a) Improvement in the gain of dual-gate FET amplifier, taking into account the second gate termination. This will increase the overall gain of the amplifier at low power levels.

(b) Use of a video amplifier with higher gain and a more sensitive crystal detector. This will remove the need for an FET amplifier in the AGC control unit and will permit the use of a 10-dB coupler. Efforts are being made to design a video amplifier which has more than 40-dB gain and a bandwidth of 300 to 400 MHz, rather than use a purchased unit for this function.

These improvements are expected to increase the dynamic range of the amplifier from -50 dBm to 0 dBm and reduce the variation in the output power level.